KG REDDY College of Engineering & Technology

DEPARTMENT

OF

ELECTRONICS AND COMMUNICATION ENGINEERING

NAME OF THE LABORATORY : DIGITAL IC APPLICATIONS
YEAR AND SEM : III B.TECH I SEM(R16)
REGULATION/LAB CODE : R16/EC056PC

DIGITAL IC APPLICATIONS LABORATORY MANUAL

HOD **PRINCIPAL**

DEPARTMENT VISION

To be recognized as a full-fledged center for learning and research in various fields of Electronics and Communication Engineering through industrial collaboration and provide consultancy for solving the real time problems

DEPARTMENT MISSION

- To inculcate a spirit of research and teach the students about contemporary technologies in Electronics and Communication to meet the growing needs of the industry.
- To enhance the practical knowledge of students by implementing projects based on real time problems through industrial collaboration

Program Outcomes(PO's):

A graduate of the Electronics and Communication Engineering Program will demonstrate:

PO1: **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2: **Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6: **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: **Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: **Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Educational Objectives (PEO's):

After 3-5 years from the year of graduation, our graduates will,

- With an exposure to the areas of VLSI, Embedded Systems, Signal / Image Processing, Communications, Wave theory, and Electronic circuits in modern electronics and communications environment.
- Demonstrate the impact of Electronics and Communications Engineering on the society, ethical, social and professional responsibilities/implications of their work.
- With strong foundations in mathematical, scientific and engineering fundamentals necessary to formulate, solve and analyze Electronics and communications. Engineering problems.
- Have strong communication inter-personal skills, multicultural adoptability and to work effectively in multidisciplinary teams.
- Engage life-long learning to become successful in their professional work.

PEO 1: To inculcate the adaptability skills into the students for design and use of analog and digital circuits and communications and any other allied fields of Electronics.

PEO 2: Ability to understand and analyze engineering issues in a broader perspective with ethical responsibility towards sustainable development.

PEO 3: To develop professional skills in students that prepares them for immediate employment and for lifelong learning in advanced areas of Electronics and communications and related fields.

PEO 4: To equip with skills for solving complex real-world problems related to VLSI, Embedded Systems, Signal/Image processing, Communications, and Wave theory.

PEO 5: Graduates will make valid judgment, synthesize information from a range of sources and communicate them in sound ways in order to find an economically viable solution.

PEO 6: To develop overall personality and character with team spirit, professionalism, integrity, and moral values with the support of humanities, social sciences and physical educational courses.

Program Specific Outcomes(PSO's)

PSO 1: **Problem Solving Skills** – Graduate will be able to apply latest electronics techniques and communications principles for designing of communications systems.

PSO 2: **Professional Skills** – Graduate will be able to develop efficient and effective Communications systems using modern Electronics and Communications engineering techniques.

PSO 3: **Successful Career** – To produce graduates with a solid foundation in Electronics and Communications engineering who will pursue lifelong learning and professional development including post graduation.

PSO 4: **The Engineer and Society**– Ability to apply the acquired knowledge for the advancement of society and self.

Course Outcomes (CO's)

Upon completion of this course, the student will be able to:

CO1: Design encoder, Comparator and Multiplexer
CO2: Plot the transform characteristics of 74H,LS, HS series IC
CO3:Desing shift registers, and counters using shift registers

R16 B.TECH ECE.

DIGITAL IC APPLICATIONS LAB

B.Tech. III Year I Sem.	L	T	P	C
Course Code: EC506PC	0	0	3	2

Note:

- To perform any twelve experiments
- Verify the functionality of the IC in the given application.

Design and Implementation of:

1. Design a 16 x 4 priority encoder using two 8 x 3 priority encoder.
2. Design a 16 bit comparator using 4 bit Comparators.
3. Design a model to 53 counter using two decade counters.
4. Design a 450 KHz clock using NAND / NOR gates.
5. Design a 4 bit pseudo random sequence generator using 4 – bit ring counter.
6. Design a 16 x 1 multiplexer using 8 x 1 multiplexer.
7. Design a 16 bit Adder / Subtractor using 4 – bit Adder / Subtractor IC's
8. Plot the transform Characteristics of 74H, LS, HS series IC's.
9. Design a 4 – bit Gray to Binary and Binary to Gray Converter.
10. Design a two Digit 7 segment display unit using this display the Mod counter output of experiment 3.
11. Design an 8 bit parallel load and serial out shift register using two 4 bit shift register.
12. Design an 8 bit Serial in and serial out shift register using two 4 bit shift register.
13. Design a Ring counter and Twisted ring counter using a 4-bit shift register
14. Design a 4 digit hex counter using synchronous one digit hex counters.
15. Design a 4 digit hex counter using Asynchronous one digit hex counters.

CONTENTS

EX1: 16×4 PRIORITY ENCODER USING 8×3 PRIORITY ENCODER

AIM: To verify the truth table of Priority Encoder

APPARATUS: ENCODER KIT

PATCH CORDS

THEORY: A priority encoder is a circuit or algorithm that compresses multiple binary inputs into a smaller number of outputs. The output of a priority encoder is the binary representation of the original number starting from zero of the most significant input bit. They are often used to control interrupt requests by acting on the highest priority encoder.

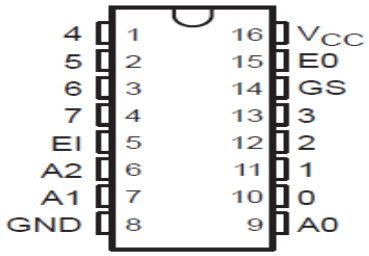
If two or more inputs are given at the same time, the input having the highest priority will take precedence. An example of a single bit 4 to 2 encoder is shown, where highest-priority inputs are to the left and "x" indicates an irrelevant value - i.e. any input value there yields the same output since it is superseded by higher-priority input. The output V indicates if the input is valid.

Priority encoders can be easily connected in arrays to make larger encoders, such as one 16-to-4 encoder made from six 4-to-2 priority encoders - four 4-to-2 encoders having the signal source connected to their inputs, and the two remaining encoders take the output of the first four as input.The priority encoder is an improvement on a simple encoder circuit, in terms of handling all possible input configurations.

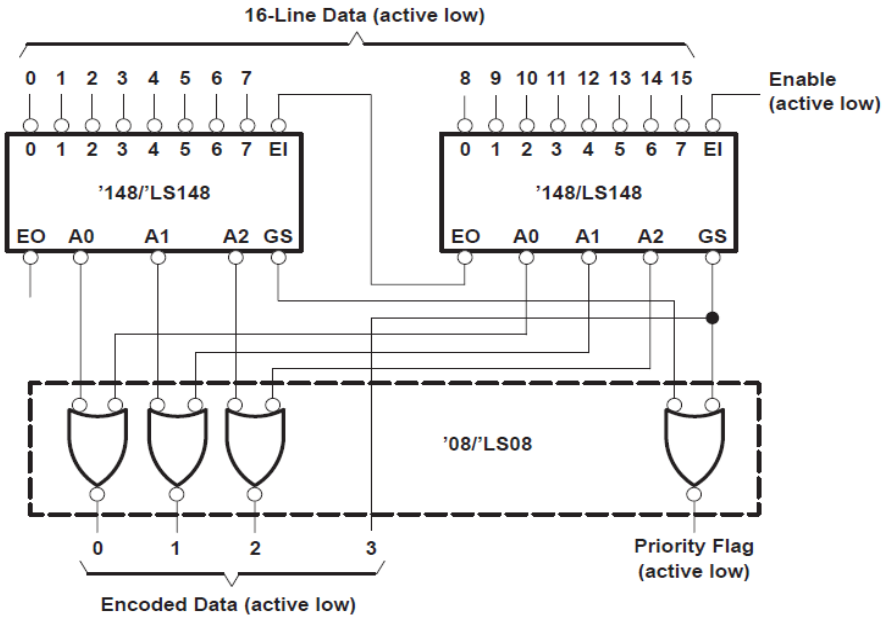
A simple encoder circuit is a one-hot to binary converter. That is, if there are 2^n input lines, and at most only one of them will ever be high, the binary code of this 'hot' line is produced on the n-bit output lines.

The **Priority Encoder** solves the problems mentioned above by allocating a priority level to each input. The priority encoders output corresponds to the currently active input which has the highest priority. So when an input with a higher priority is present, all other inputs with a lower priority will be ignored.

PIN DIAGRAM:



CIRCUIT DIAGRAM:



TRUTH TABLE:

Encoder Data (Active Low):

Inputs															EI	Outputs			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	3	2	1	0
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	0	0	0	0
H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	0	0	0	1
H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	0	0	1	0
H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	0	0	1	1
H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	0	1	0	0
H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	0	1	0	1
H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	0	1	1	0
H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	0	1	1	1
H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	1	0	0	0
H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	1	0	0	1
H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	1	0	1	0
H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	1	0	1	1
H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	1	1	0	0
H	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	1	1	0	1

H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	L	1	1	1	0
H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	1	1	1	1

PROCEDURE:

1. Make Connections as per the above Circuit Diagram
2. 0 to 15 Inputs are Connected to Inputs Switches
3. Connect EI (Pin no. 5) of 1st Encoder to E0 (Pin no.15) of 2nd Encoder
4. Connect A0,A1,A2 (Pin no.s 9,7,6) of 1st Encoder to Inputs of Three AND (74LS08) Gate.
5. Connect A0,A1,A2 (Pin no.s 9,7,6) of 2nd Encoder to Inputs of Three AND (74LS08) Gate.
6. Connect GS (Pin no.14) of Both Encoders to the Input of Fourth AND (74LS08) Gate.
7. Connect Outputs of Three AND (74LS08) Gates to Connect Output Switches
8. Connect GS (Pin no.14) of 2nd Encoder to Output Switch
9. Give Inputs as per the Truth Table & Observe Output.

Result: Hence verified the truth table of Priority Encoder.

Viva Questions:

1. Define encoder
2. Define decoder
3. How many number of inputs and outputs for the encoder
4. How many number of inputs and outputs for the DECODER
5. Number of inputs for decimal to BCD encoder

EX2: 16 BIT COMPARATOR USING 4 BIT COMPARATORS

AIM: To verify the truth table of 4-bit Comparator.

APPARATUS: COMPARATOR KIT
PATCH CORDS

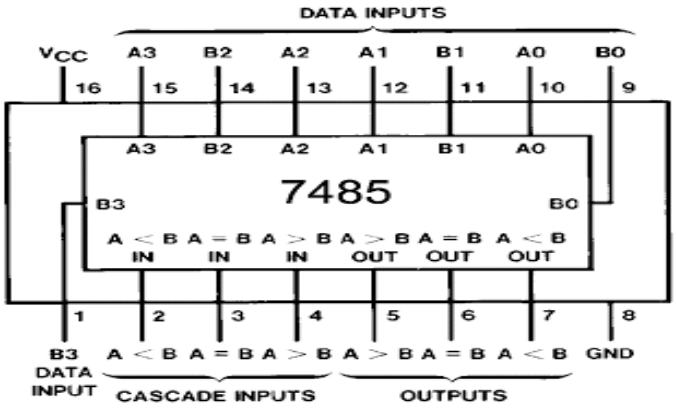
THEORY :

The SN54/74LS85 is a 4-Bit Magnitude Camparator which compares two 4-bit words (A, B), each word having four Parallel Inputs ($A_0 - A_3$, $B_0 - B_3$); A_3, B_3 being the most significant inputs. Operation is not restricted to binary codes, the device will work with any monotonic code. Three Outputs are provided: "A greater than B" ($O_{A>B}$), "A less than B" ($O_{A<B}$), "A equal to B" ($O_{A=B}$). Three Expander Inputs, $I_{A>B}$, $I_{A<B}$, $I_{A=B}$, allow cascading without external gates. For proper compare operation, the Expander Inputs to the least significant position must be connected as follows: $I_{A<B} = I_{A>B} = L$, $I_{A=B}$ = H. For serial (ripple) expansion, the $O_{A>B}$, $O_{A<B}$ and $O_{A=B}$ Outputs are connected respectively to the $I_{A>B}$, $I_{A<B}$, and $I_{A=B}$ Inputs of the next most significant comparator, as shown in Figure 1. Refer to Applications section of data sheet for high speed method of comparing large words.

The Truth Table on the following page describes the operation of the SN54/74LS85 under all possible logic conditions. The upper 11 lines describe the normal operation under all conditions that will occur in a single device or in a series expansion scheme. The lower five lines describe the operation under abnormal conditions on the cascading inputs. These conditions occur when the parallel expansion technique is used.

- Easily Expandable
- Binary or BCD Comparison
- $O_{A>B}$, $O_{A<B}$, and $O_{A=B}$ Outputs Available

PIN DIAGRAM :



TRUTH TABLE:

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3,B3	**A2,B2**	**A1,B1**	**A0,B0**	**A>B**	**A<B**	**A=B**	**A>B**	**A<B**	**A=B**
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L

PROCEDURE:

1. Connect Inputs (A0,A1,A2,A3,B0,B1,B2,B3) to Input Switches
2. Connect Cascade Inputs (A<B,A>B,A=B) to Input Switches
3. Connect Outputs (A<B,A>B,A=B) to Output Switches
4. Observe the Truth Table.

Result: Verified the truth table of Comparator.

Viva Questions:

1. What is comparator?

2. design 2bit comparator using logic gates

3 number of outputs for the comparator?

EX3: MODULO N COUNTER USING DECADE COUNTER

AIM: To Verify The Truth Table Of Decade Counter.

APPARATUS: DECADE Counter Kit
PATCH CORDS

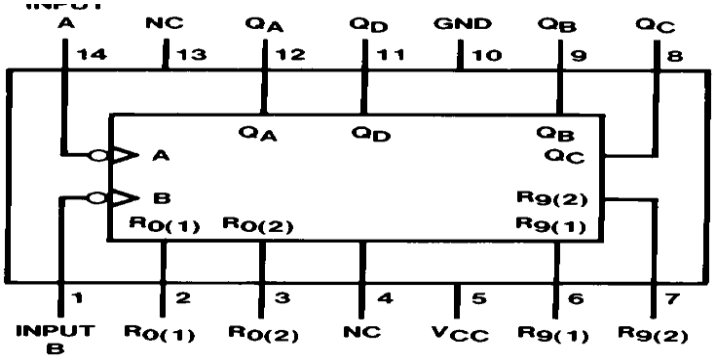
THEORY:

The counters four outputs are designated by the letter symbol Q with a numeric subscript equal to the binary weight of the corresponding bit in the BCD counter circuits code. So for example Q_A, Q_B, Q_C and Q_D. The 74LS90 counting sequence is triggered on the negative going edge of the clock signal, that is when the clock signal CLK goes from logic 1 (HIGH) to logic 0 (LOW).

The additional input pins R_1 and R_2 are counter "reset" pins while inputs S_1 and S_2 are "set" pins. When connected to logic 1, the Reset inputs R_1 and R_2 reset the counter back to zero, 0 (0000), and when the Set inputs S_1 and S_2 are connected to logic 1, they Set the counter to maximum, or 9 (1001) regardless of the actual count number or position.

As we said before, the 74LS90 counter consists of a divide-by-2 counter and a divide-by-5 counter within the same package. Then we can use either counter to produce a divide-by-2 frequency counter only, a divide-by-5 frequency counter only or the two together to produce our desired divide-by-10 BCD counter. With the four flip-flops making up the divide-by-5 counter section disabled, if a clock signal is applied to input pin 14 (CLK_A) and the output taken from pin 12 (Q_A), we can produce a standard divide-by-2 binary counter for use in Pin Diagram circuits as shown below.

Pin Diagrams of 7490 IC is as below:



TRUTH TABLE:

Reset I/p				Outputs			
RESET0 (pin 2)	**RESET0 (pin 3)**	**R3**	**R2**	**Qd**	**Qc**	**Qb**	**Qa**
H	**H**	**L**	**X**	**L**	**L**	**L**	**L**
H	**H**	**X**	**L**	**L**	**L**	**L**	**L**
X	**X**	**H**	**H**	**H**	**L**	**L**	**H**
X	**L**	**X**	**L**	**COUNT**			
L	**X**	**L**	**X**	**COUNT**			
L	**X**	**X**	**L**	**COUNT**			
X	**L**	**L**	**X**	**COUNT**			

PROCEDURE:

1. Connect inputs RESET0(pin 2), RESET0(pin 3), R3, R2 to the input switches and Qa, Qb, Qc, Qd to the output switches.
2. Connect $\overline{\text{Clock A}}$ to clock pulse.
3. Connect $\overline{\text{Clock B}}$ to Qa.
4. Feed the logic signals either H/L as shown in the truth table.
5. Monitor the outputs Qa, Qb, Qc, Qd.
6. Verify the truth table.

Result: Hence verified the truth table of Decade Counter.

Viva Questions:

1. What is decade counter?

2. what is the maximum count for decade counter?

3. pin diagram of 74ls90?

EX4: 16:1 MUX USING 8:1 MUX

AIM: To verify the truth table of Multiplexer.

APPARATUS: MULTIPLEXER kit
PATCH CORDS.

THEORY:

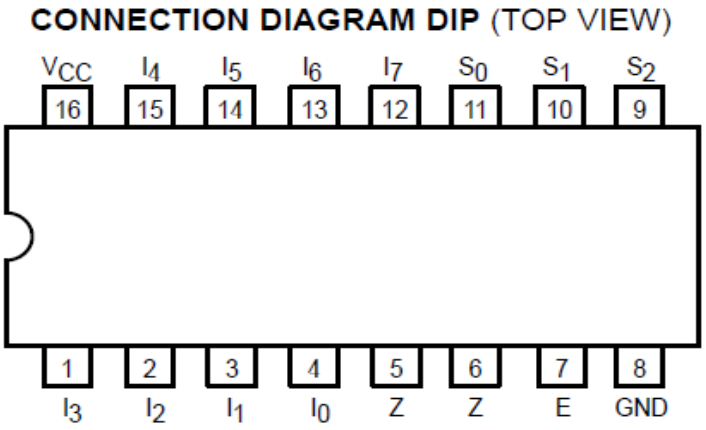
TTL/MSI SN54/74LS151 is a high speed 8-input Digital Multiplexer.
It provides, in one package, the ability to select one bit of data from up to eight sources. The LS151 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

- Schottky Process for High Speed
- Multifunction Capability
- On-Chip Select Logic Decoding
- Fully Buffered Complementary Outputs
- Input Clamp Diodes Limit High Speed Termination Effects

FUNCTIONAL DESCRIPTION

The LS151 is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S0, S1, S2. Both assertion and negation outputs are provided. The Enable input (E) is active LOW. When it is not activated, the negation output is HIGH and the assertion output is LOW regardless of all other inputs.

PIN DIAGRAM



$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

PROCEDURE:

1. Connect Inputs S2,S1,S0,I0, I1,I2,I,3 I4,I5,I6, I7 and Enable (E) to Logic Input Sockets.
2. Connect Output terminal Z & $\overline{Z}$ to Logic Output Sockets.
3. Verify output with given Truth Table.

Result: Hence verified the truth table of Multiplexer.

Viva Questions:

1. What is Mux?

2. Define Demux?

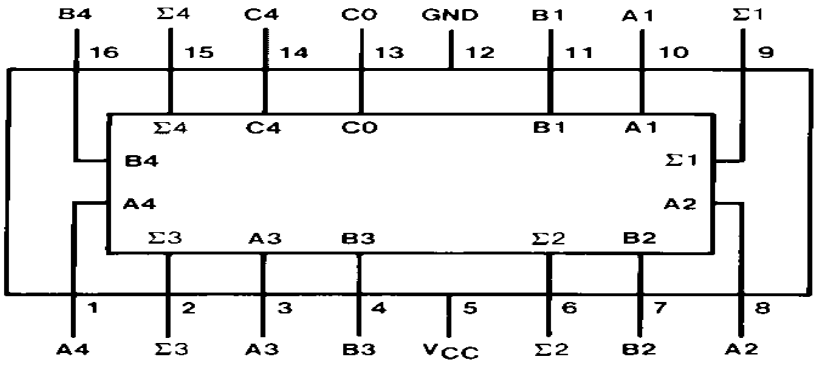
3. Design 4:1 mux using logic gates and write the equation

-EX5: ADDER/SUBTRACTOR

AIM: To verify the Adder function.

APPARATUS: ADDER/SUBTRACTOR kit
PATCH CORDS

PIN DIAGRAM:



TRUTH TABLE:

INPUTS									OUTPUTS				
Cin	**A0**	**A1**	**A2**	**A3**	**B0**	**B1**	**B2**	**B3**	**S0**	**S1**	**S2**	**S3**	**OUT**
0	0	0	0	1	1	0	0	1	1	0	0	0	1
1	0	0	0	1	1	0	0	1	0	1	0	0	1

NOTE: You may add any two 4-bit binary numbers by making the cin to logic 0/1.

PROCEDURE:

1. Connect the inputs A0, A1, A2, A3, B0, B1, B2, B3 and Cin to the input switches.(A0-A3 represents 1binary input and B0-B3 represents another binary input, Cin represents carry input)
2. Connect the Outputs S0, S1, S2, S3 and C4 (0ut on the board) to the output switches.
3. Feed the logic inputs and note down the outputs.

NOTE:

1. When the Cin is at logic 0, the output will be displaying the carry output but doesn't add with the binary inputs given.
2. When the Cin is at logic 1, the Output will be displayed by adding the carry.

Result: Hence Performed the 4-bit Binary Addition using IC 7483.

Viva Questions:

1. What is adder?
2. Sum equation of 1-bit full adder
3. Carry equation of 1-bit full adder
4. General sum and carry equation

EX6: CODE CONVERTER 4-BIT GRAY TO BINARY AND BINARY TO GRAY CODE CONVERTER KIT

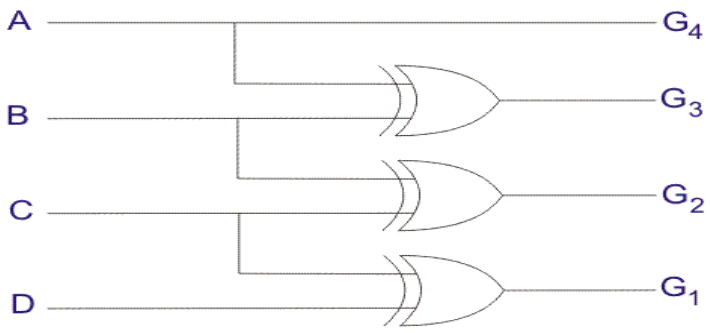
AIM: Observe Binary to Gray & Gray to Binary Code Conversion.
APPARATUS: GRAY-BINARY-GRAY Kit
Patch Cords

THEORY :

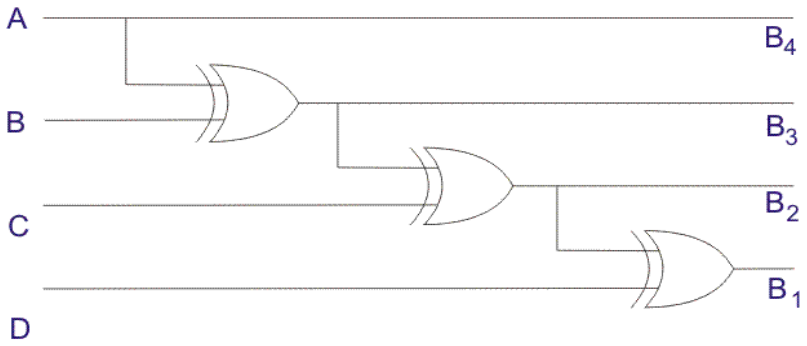
The logical circuit which converts binary code to equivalent gray code is known as **binary to gray code converter.** The gray code is a non weighted code. The successive gray code differs in one bit position only that means it is a unit distance code. It is also referred as cyclic code. It is not suitable for arithmetic operations. It is the most popular of the unit distance codes. It is also a reflective code. An n-bit Gray Code can be obtained by reflecting an n-1 bit code about an axis after 2^{n-1} rows, and putting the MSB of 0 above the axis and the MSB of 1 below the axis.

In **gray to binary code converter**, input is a multiplies gray code and output is its equivalent binary code. Let us consider a 4 bit gray to binary code converter. To design a 4 bit gray to binary code converter, we first have to draw a conversion table.

CIRCUIT DIAGRAM:



Logic Circuit for Binary to Gray Code Converter



Logic Circuit for Gray to Binary Code Converter

TRUTH TABLE:

INPUTS				OUTPUTS			
BINARY CODE				GRAY CODE			
A	B	C	D	G1	G2	G3	G4
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

INPUTS				OUTPUTS			
GRAY CODE				BINARY CODE			
A	B	C	D	B4	B3	B2	B1
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1

PROCEDURE:

BINARY TO GRAY:

1. Connect Inputs (A,B,C,D) to Input Switches (Red LED)
2. Connect Outputs (G1,G2,G3,G4) to Output Switches (Green LED)
3. Give Binary Inputs at A,B,C,D & Observe Gray Code Outputs as per Truth Table.

GRAY TO BINARY:

1. Connect Inputs (A,B,C,D) to Input Switches (Red LED)
2. Connect Outputs (B1,B2,B3,B4) to Output Switches (Green LED)
3. Give Gray Code Inputs at A,B,C,D & Observe Binary Code Outputs as per Truth Table.

Result: Binary to Gray & Gray to Binary Code Conversion is Verified.

Viva Questions:

1. What is Binary ?
2. Decimal code?
3. Explain binary to Decimal code converter
4. Explain Decimal to binary code converter

EX7: BCD TO 7 SEGMENT DISPLAY

AIM: To verify the truth table of BCD to 7 Segment Display

APPARATUS: BCD/7 SEGMENT Kit
PATCH CORDS

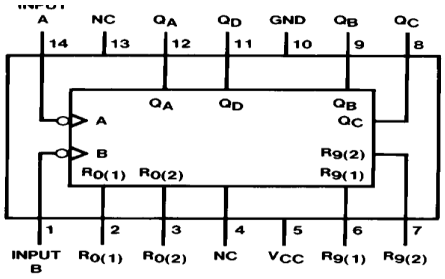
THEORY:

The counters four outputs are designated by the letter symbol Q with a numeric subscript equal to the binary weight of the corresponding bit in the BCD counter circuits code. So for example, Q_A, Q_B, Q_C and Q_D. The 74LS90 counting sequence is triggered on the negative going edge of the clock signal, that is when the clock signal CLK goes from logic 1 (HIGH) to logic 0 (LOW).

The additional input pins R_1 and R_2 are counter "reset" pins while inputs S_1 and S_2 are "set" pins. When connected to logic 1, the Reset inputs R_1 and R_2 reset the counter back to zero, 0 (0000), and when the Set inputs S_1 and S_2 are connected to logic 1, they Set the counter to maximum, or 9 (1001) regardless of the actual count number or position.

As we said before, the 74LS90 counter consists of a divide-by-2 counter and a divide-by-5 counter within the same package. Then we can use either counter to produce a divide-by-2 frequency counter only, a divide-by-5 frequency counter only or the two together to produce our desired divide-by-10 BCD counter.With the four flip-flops making up the divide-by-5 counter section disabled, if a clock signal is applied to input pin 14 (CLK_A) and the output taken from pin 12 (Q_A), we can produce a standard divide-by-2 binary counter for use in Pin Diagram circuits as shown below.

Pin Diagrams of 7490 IC is as below:



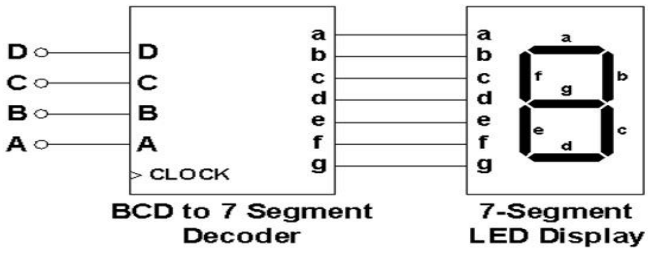
PROCEDURE:

1. Connect inputs RESET0(pin 2), RESET0(pin 3), R3, R2 to the input switches and Qa, Qb, Qc, Qd to the output switches.
2. Connect Clock A to clock pulse.
3. Connect Clock B to Qa.
4. Feed the logic signals either H/L as shown in the truth table.
5. Monitor the outputs Qa, Qb, Qc, Qd.
6. Verify the truth table.

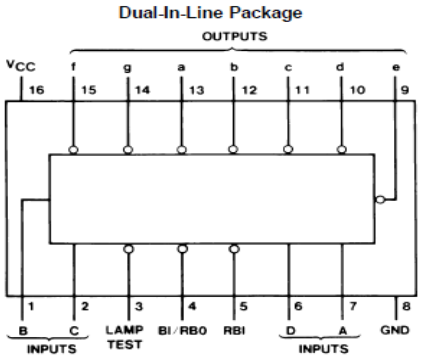
TRUTH TABLE:

Reset I/p				Outputs			
RESET 0 (PIN 2)	RESET 0 (PIN 3)	R3	R2	Qd	Qc	Qb	Qa
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

BCD COUNTER TO 7 SEGMENT DISPLAY:



Connection Diagram

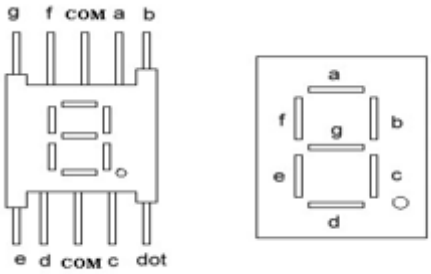


PROCEDURE:

1. Connect BCD Outputs(Qa, Qb, Qc, Qd) to 7 Segment Display (A,B,C,D).

2. a,b,c,d,e,f,g Connections are Internally Connected.
3. Verify the Count Outputs 0,1,2,3,4,5,6,7,8,9

7 SEGMENT DISPLAY:



Seven-Segment Display

THEORY:

The Light Emitting Diode (LED) finds its place in many applications in these modern electronic fields. One of them is the Seven Segment Display. Seven-segment displays contains the arrangement of the LEDs in "Eight" (8) passion, and a Dot (.) with a common electrode, lead (Anode or Cathode). The purpose of arranging it in that passion is that we can make any number out of that by switching ON and OFF the particular LED's. Here is the block diagram of the Seven Segment LED arrangement.

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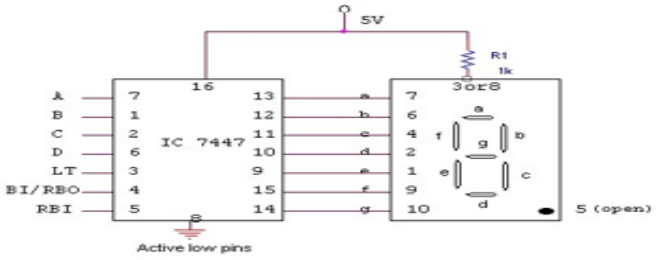
A decoder is a combinational circuit that connects the binary information from 'n' input lines to a maximum of 2^n unique output lines. The IC7447 is a BCD to 7-segment pattern converter. The IC7447 takes the Binary Coded Decimal (BCD) as the input and outputs the relevant 7 segment code.

CIRCUIT DIAGRAM:



TRUTH TABLE:

BCD Inputs				Output Logic Levels from IC 7447 to 7-segments							Decimal number display
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	1	0	0	1	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0	2
0	0	1	1	0	0	0	0	1	1	0	3
0	1	0	0	1	0	0	1	1	0	0	4
0	1	0	1	0	1	0	0	1	0	0	5
0	1	1	0	1	1	0	0	0	0	0	6
0	1	1	1	0	0	0	1	1	1	1	7
1	0	0	0	0	0	0	0	0	0	0	8
1	0	0	1	0	0	0	1	1	0	0	9

PROCEDURE:

1. Connect Inputs A,B,C,D to Input Switches (RED LED)
2. Connect 7-Segment Outputs(a,b,c,d,e,f,g) to Output Switches (GREEN LED)
3. Verify the Truth Table and observe the outputs.

Result: Hence verified the truth table of BCD to 7 Segment Display

Viva Questions:

1. What is 7 segment display

2. explain the equations for all the inputs of 7 segment

EX8: UNIVERSAL SHIFT REGISTER

AIM: To Verify the Truth Table of Universal Shift Register.

APPARATUS: Universal Shift Register Trainer kit With ICs-74194

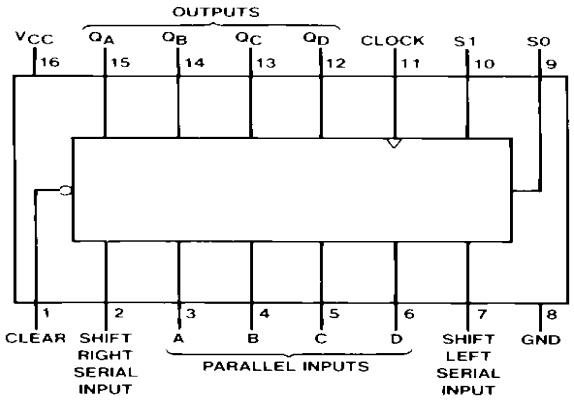
Patch chords,

Clock Pulse Generator.

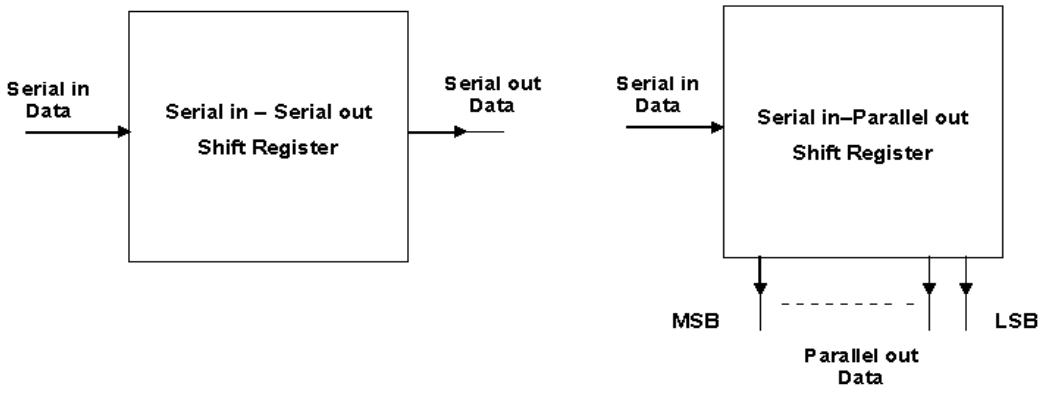
THEORY:

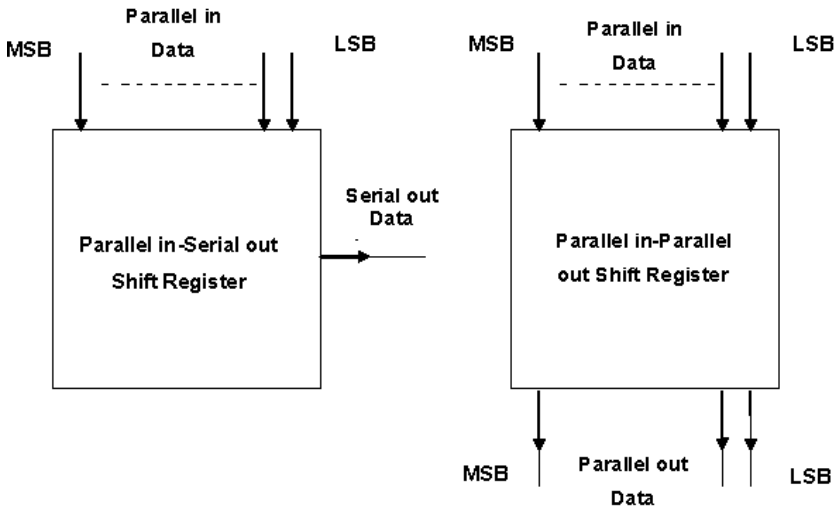
A register is simply a group of flip flops that can be used to store a binary number. A shift register is a group of flip flops connected such that the binary number can be entered (shifted) into the register and possibly shifted out. There are two ways to shift the data (bits in the binary number) from one place to another. The first method involves shifting the data 1bit at a time in a serial fashion, beginning with either MSB or LSB. This technique is referred to as serial shifting. The second method involves shifting all the data bits simultaneously and is referred to as parallel shifting. There are two ways to shift data into a register (serial or parallel) and similarly two ways to shift data out of the register. This leads to the construction of four basic types of registers.

1. Serial in – Serial out shift register.
2. Serial in – Parallel out shift register.
3. Parallel in – Serial out shift register.
4. Parallel in – Parallel out shift register.



Block diagram of 4 types of shift registers (n-bit).





TRUTH TABLE:

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				QA	QB	QC	QD
	S1	S0		LEFT	RIGHT	A	B	C	D				
H	X	X	⌞	X	X	X	X	X	X	QA0	QB0	QC0	QD0
H	H	H	⌐	X	X	a	b	c	d	a	b	c	d
H	L	H	⌐	X	H	X	X	X	X	H	QAn	QBn	QCn
H	L	H	⌐	X	L	X	X	X	X	L	QAn	QBn	QCn
H	H	L	⌐	H	X	X	X	X	X	QBn	QCn	QDn	H
H	H	L	⌐	L	X	X	X	X	X	QBn	QCn	QDn	L
H	L	L	X	X	X	X	X	X	X	QA0	QB0	QC0	QD0

PROCEDURE:

1. Derive the wiring diagram.
2. Connect Input terminals to the Logic Input Sockets.
   S1, S0, SERIAL LEFT, SERIAL RIGHT, PARALLEL DATA - A, B, C and D to Logic Input Sockets.
3. Connect CLEAR to VCC.
4. Connect External Clock to the CLOCK Terminal.
5. Connect QA, QB, QC and QD to the Logic Output terminals.
6. Observe output changes at O/P Terminals with given Truth Table.

Result: Verified the Truth Table of Universal Shift Register.

Viva Questions:

1. What is shift resister

2. Explain PIPO,SIPO,SISO and SIPO

EX9: PSEUDO RANDOM SEQUENCE GENERATOR

(4-BIT) RING COUNTER

AIM: To verify the 4-bit Ring Counter.

APPARATUS: Ring Counter Kit , Patch Cards

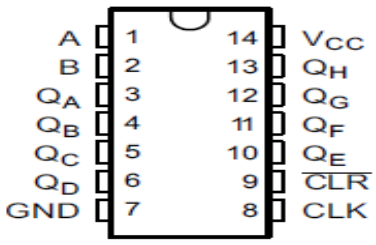
THEORY:

In the Shift register if we apply a serial data signal to the input of a serial-in to serial-out shift register, the same sequence of data will exit from the last flip-flip in the register chain after a preset number of clock cycles thereby acting as a sort of time delay circuit to the original signal.But what if we were to connect the output of this shift register back to its input so that the output from the last flip-flop, Q_D becomes the input of the first flip-flop, D_A. We would then have a closed loop circuit that "re-circulates" the DATA around a continuous loop for every state of its sequence, and this is the principal operation of a **Ring Counter.** Then by looping the output back to the input, we can convert a standard shift register into a ring counter. Consider the circuit below.

The synchronous **Ring Counter** example above is preset so that exactly one data bit in the register is set to logic "1" with all the other bits reset to "0". To achieve this, a "CLEAR" signal is firstly applied to all the flip-flops together in order to "RESET" their outputs to a logic "0" level and then a "PRESET" pulse is applied to the input of the first flip-flop (FFA) before the clock pulses are applied. This then places a single logic "1" value into the circuit of the ring counter.

So on each successive clock pulse, the counter circulates the same data bit between the four flip-flops over and over again around the "ring" every fourth clock cycle. But in order to cycle the data correctly around the counter we must first "load" the counter with a suitable data pattern as all logic "0's" or all logic "1's" outputted at each clock cycle would make the ring counter invalid.This type of data movement is called "rotation", and like the previous shift register, the effect of the movement of the data bit from left to right through a ring counter can be presented graphically as follows along with its timing diagram.

4-bit Ring Counter:



PROCEDURE:

1. Connect I/P A,B & CLR to the input switches,CLK to the pulsar switch.
2. Connect the outputs QA, QB, QC, and QD to the output switches.
3. First make the clear input high, then make both input A & B high
4. Now give the clock pulse, for every pulse the output shifts from one flip flop to another.

NOTE: When you are giving the clear input high all the outputs may not become zero and hence count continues in the same manner.

Result: Hence the 4-bit Ring Counter is Verified.

Viva Questions:

1. What is counter
2. What is ring counter

EX10: 4 –BIT SYNCHRONOUS COUNTER

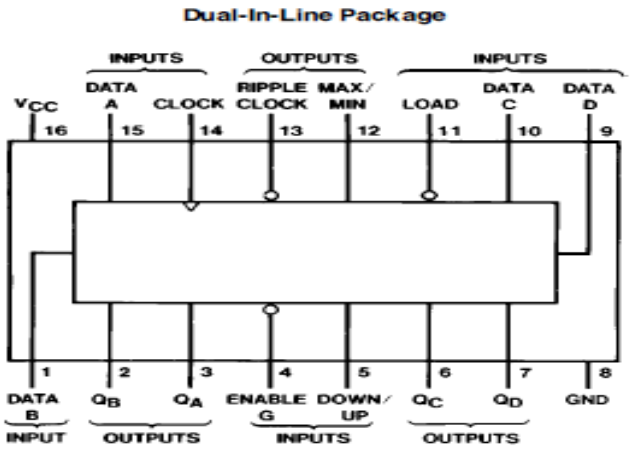
AIM: To verify the truth table of 4-bit Synchronous Counter.

APPARATUS: COUNTER Kit
PATCH CORDS

THEORY:

A counter is a register capable of counting number of clock pulse arriving at its clock input. Counter represents the number of clock pulses arrived. An up/down counter is one that is capable of progressing in increasing order or decreasing order through a certain sequence. An up/down counter is also called bidirectional counter. Usually up/down operation of the counter is controlled by up/down signal. When this signal is high counter goes through up sequence and when up/down signal is low counter follows reverse sequence.

CONNECTION DIAGRAM:



PROCEDURE:

1. Connect the inputs A, B, C, D, G, max/min,load and up/down to the logic input switches and outputs Qa Qb, Qc and Qd to the output logic switches.
2. Keep load input high.
3. When up input (on the board) is fed with logic 0 then the count is “Up” count.
4. When up input (on the board) is fed with logic 1 then the count is “down” count.
5. This Count is achieved with Pulsar switch (instead of the clock, pulsar input has to be connected and the output changes with every pulse).

FUNCTION TABLE: (UP COUNT)

COUNT	OUTPUTS			
	Qd	Qc	Qb	Qa
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

COUNT	OUTPUTS			
	Qd	Qc	Qb	Qa
0	H	H	H	H
1	H	H	H	L
2	H	H	L	H
3	H	H	L	L
4	H	L	H	H
5	H	L	H	L
6	H	L	L	H
7	H	L	L	L
8	L	H	H	H
9	L	H	H	L
10	L	H	L	H
11	L	H	L	L
12	L	L	H	H
13	L	L	H	L
14	L	L	L	H
15	L	L	L	L

NOTE:

All the inputs connected may be high or low.They are just connected to close the circuit. For every count pulse should be given then only the output changes.

Result: Hence verified the truth table of 4-Bit Synchronous , Binary Counter.

Viva Questions:

1. Explain up counter
2. Explain down counter
3. Synchronous counter

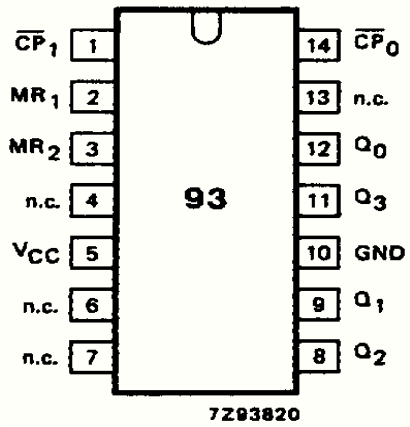
EX11: 4-BIT ASYNCHRONOUS COUNTER

AIM: To Verify The Truth Table Of 4 Bit Asynchronous Counter.

APPARATUS: MTS-COUNTER
PATCH CORDS

THEORY: A 4-Bit Asynchronous Counter Count From 0 To 15. To Implement Binary Counter We Require 7493 IC. Pin Diagram Of These IC Is As Below.

PIN CONFIGURATION OF 74HCT93 :



PROCEDURE:

1. Connect The Inputs MR1, MR2, To The Logic Input Switches And Outputs Qo, Q1, Q2, And Q3 To The Logic Outputs.
2. Feed The Logic Signals 0 Or 1 As Shown In The Truth Table.
3. Monitor The Outputs Q0, Q1, Q2, Q3.
4. Verify The Truth Table.

NOTE:

1. Connect $\overline{CP1}$ To Qo
2. Pulse Input Is Connected To Pin 14 ($\overline{CP0}$)
3. When The Count Output Is Present Count Can Be Observed With Every Pulse.(16 Pulses)

TRUTH TABLE:

Reset I/P		Outputs			
MR1	**MR2**	**Q3**	**Q2**	**Q1**	**Q0**
H	H	L	L	L	L
L	H	COUNT			
H	L	COUNT			
L	L	COUNT			

COUNT TABLE:

COUNT	OUTPUTS			
	Q3	**Q2**	**Q1**	**Q0**
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Result: Hence Verified The Truth Table Of 4 Bit Binary Asynchronous Counter.

Viva Questions:

1. What is Asynchronous counter?