Mr. Bavusaheb Kunchanur

Faculty Id	:	6931-161213-120958
Date of Birth	:	12/05/1989
Designation	:	Assistant Professor
Years of Experience	:	Teaching : 1.7 years
		Industry : 1.8 years
Email Id	:	bavusaheb@kgr.ac.in
Phone Number	:	9611657428
UG Degree	:	B.E in Electronics and Communication Engineering, BLDCET,Bijapur, VTU,Karnataka
PG Degree	:	M.Tech in VLSI Design and Embedded systems,MITE,Moodbidre, VTU, Karnataka
Employment Status	:	Full Time - Ratified by JNTUH
Areas of Specialization	:	• Low power VLSI • Embedded system • IoT • Physical Disign • Digital Design
UG Subjects Taught	:	Linear and Digital IC applications, VLSI design, Radar Systems, Digital logic Design, Switching theory and logic design, Linear IC's.
Projects handled	:	➢ **PROJECT ORIENTED INTERNSHIP -INDIAN TELEPHONE INDUSTRY (ITI)** BANGALORE 24.08.2015 TO 23.11.2015. ✓ Worked on communication protocols in R&D department ✓ Done a project on communication protocols using VHDL ✓ Worked on encryption and decryption of communication protocols Got hands on training on Xilinx vivado

- **Design and Analysis of 16-bit Efficient Carry Select Adder using Full Swing modified GDI Techniques:**

Area, power and delay are important factors in VLSI design. In order to reduce these factors several authors proposed several techniques, one of such technique is Gate Diffusion Input (GDI). Although GDI technique reduces area, it suffers from swing degradation problem. The conventional GDI technique is modified in order to achieve full swing. Three different approaches are proposed and 16 bit carry select adder is designed using these models. Area, power and delay are compared.

Design and Simulation of Communication Protocols using VHDL: VHDL modules are designed for I2C protocol, SPI protocol and UART protocols. Vhdl code is designed and simulated using Xilinx ISE v10.2

Papers Published:

International Journals

- ✓ "Speaking System For Mute People Using Raspberry Pi", International Journal of Emerging Technologies and Innovative Research (www.jetir.org), ISSN:2349-5162, Vol.5, Issue 5, page no.679-685, MAY-2018, Available :http://www.jetir.org/papers/JETIR1805715.pdf
- ✓ "Design and analysis of vedic multiplier using full swing modified gate defused input method", IJCRT, page 301-306, vol-6,Issue-1,December 2017.**http://www.ijcrt.org/IJCRTNCES047.pdf**
- ✓ "Outline of re-enactment distinction CMOS Phase Frequency Detectors for rapid and low jitter PLL", IJCRT, page 246-251, vol-6,Issue-1,December 2017. http://www.ijcrt.org/papers/IJCRTNCES038.pdf
- ✓ "Design and analysis of carry select adder using modified full swing GDI techniques" IJRASET page no. 67-72, vol-2 Issue 5, may 2016 http://www.ijraset.org/papers/IJRASET0155.pdf
- ✓ "Design and analysis of full adder using different low power techniques" American journal of computer science and information technology, vol 4 issue 1, may 2016
- ✓ "Comparative study and analysis of different low power design styles", IJSER page no. 12-16, vol-1 jan-2016
- ✓ "design and analysis of 1-bit hybrid full adders" IJAR vol-1 Issue 2 jan 2016 page no.3-6.
- ✓ "Design and analysis of full adder using different low power techniques" Pubicon publication, page no. 16-19, April 2016

Papers reviewed as Reviewer

- *"A Phase Frequency Detector for a High Frequency PLL Design", JETIR182966,Journal of Emerging Technologies and Innovative Research(JETIR), ISSN: 2349-5162 | Impact Factor: 5.87.*
- *"Processing And Analysis Of Digital images And Checking The Quality Of Data Captured", JETIR18303, Journal of Emerging Technologies and Innovative Research(JETIR), ISSN: 2349-5162 | Impact Factor: 5.87.*

Membership:

- Reviewer Board member in Journal of Emerging Technologies and Innovative Research(JETIR), ISSN: 2349-5162 | Impact Factor: 5.87, ID-113271
- Reviewer Board member in International Journal of Creative Research Thoughts (IJCRT) ISSN: 2320-2882. Member ID-113271

Workshops attended:

- Attended 6 days FDP on "VLSI circuits and systems" conducted in coordination with UGC HRDC
- Attended 5 days FDP on "Digital VLSI design using verilog" conducted by CDAC and TASK
- Attended 2 days workshop on NPTEL videos and courses conducted by IIT Madras
- Attended FDP on Recent Trends in Engineering Education.
- Attended FDP on Out Come Based Education System.
- Attended FDP on Active Learning Methods.
- Attended Two National level Conferences at KGRCET

Achievement/ Certification course

- NPTEL Elite certificate for "VLSI Physical design", September 2017
- CDAC certification for "Digital VLSI Design", Dec 2017
- Won best paper in national conference NCESTFOSS held in KGRCET, Hyderabad.
- Won 2nd prize in PG technical symposium on 13th may 2016 in SDIT Mangalore.
- Conducted 2 days hands on training on "Introduction to Arduino and embedded system" in Secab engineering college, Bijapur
- Guided 2 Project groups for "Smart India Hackathon 2017"
- Handled two days workshop on Xilinx ISE in MITE, Moodabidri
- Handled three days workshop on Mentor graphics, in MITE, Moodbidri