PAGADALA USHA

Faculty Id	:	4110-150413-130923
Date of Birth	:	25 April , 1989
Designation	:	Assistant Professor
Years of Experience	:	Teaching : 4.6 years
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Employment Status	:	Full Time - Ratified by JNTUH
Areas of Specialization	:	• VLSI system Design
UG Degree	:	Electronics and Communication Engineering,2010,SVEC,Suryapet, Telangana
PG Degree	:	VLSI System Design, 2014, VNR VJIET, Hyderabad, Telangana.
UG Subjects Taught	:	• Microwave and engineering(MWE) • Radar systems(RS) • Electronic circuit analysis(ECA) • Electronic devices and circuits(EDC) • Digital signal processing(DSP) • Switching theory and logic design(STLD) • Analog Electronics(AE)

Conferences and Papers Publications:

- Presented a paper in National Conference on Recent Trends In Engineering Education and Significance of Free Open Source Software(NCESTFOSS-2017) on "OUTLINE OF REENACTMENT DISTINCTION CMOS PHASE FREQUENCY DETECTORS FOR RAPID AND LOW JITTER PLL" organized by KGRCET.(http://www.ijcrt.org/papers/IJCRTNCES038.pdf)
- Presented a paper in National Conference on Recent Trends In Engineering Education and Significance of Free Open Source Software(NCESTFOSS-2017) on "Design And Analysis Of Vedic Multiplier Using Full Swing Modified Gate Defused Input Method" organized by KGRCET. (http://www.ijcrt.org/papers/IJCRTNCES047.pdf)
- Presented a paper in National Conference on Recent Trends In Engineering Education and Significance of Free Open Source Software(NCRTEEFOSS-2016) on "VLSI implementation of fast addition using quaternary signed digit number system" organized by KGRCET. (http://ijiet.com/wp-content/uploads/2016/12/1130.pdf)
- Published the journal in International Journal Of Science Engineering and Technology(IJSET) on "An efficient implementation of automatic washing machine control system using verilog"(ISSN 2348-4098,Volume-2, Issue-7,Sept-Oct 2014,Pages:1575 -1578). (http://www.ijset.in/wp-content/uploads/2014/11/IJSET.1020141026.1011.2910_P_1575-1578.pdf)
- Published the journal in International Journal of Advanced Technology and Innovative Research(IJATIR) on "Visual cryptography for color images using error diffusion" (ISSN 2348-2370,Volume-6, Issue-3,April-2014,Pages:124-131). (http://www.ijatir.org/uploads/516324IJATIR843-18.pdf)
- Presented a paper in International Conference on Paradigms in Engineering& Technology(ICPET 2016) on "An efficient low power cross coupled SRAM using Schmitt trigger principle" organized by Methodist college of engineering and technology, Hyderabad.
- Published a paper in international journal of innovative technologies(IJITECH) on "Fall Detection and Observation System Over Linux Environment with IOT" (ISSN 2321-8665,Volume-03,Issue-06,August-2015,Pages: 0901-0904). (http://ijitech.org/uploads/162534IJIT6191-165.pdf)
- Published a paper in international journal of innovative technologies(IJSETR) on " Implementation Of A Home Embedded Surveillance Device with Majority Voting Mechanism" (ISSN 2319-8885,Volume-04,Issue-50,December-2015,Pages: 10869-10872). (http://ijsetr.com/uploads/365142IJSETR8016-1875.pdf)
- Published a paper in International Journal of Scientific Engineering and Technology Research(IJSETR) on "Mathematical Modeling And FPGA Implementation of Particle Swarm Optimization" (ISSN 2319-8885,Volume-2, Issue-17,November-2013,Pages:2003-2007). (http://www.ijsetr.com/uploads/643215IJSETR496-18.pdf)

Papers reviewed as Reviewer

1. ***Reviewer in Fourth International Conference On Transformations in Engineering Education (ICTIEE-2017).***
2. ***Reviewer in Fifth International Conference On Transformations in Engineering Education (ICTIEE-2018).***

Workshops attended:

- Faculty Development Program on EFFECTIVE TEACHING AND LEARNING at KGRCET, held on 14th may to 18th may, 2018.
- Faculty Development Program on VLSI SYSTEM DESIGN at MLR Engineering College held on 28TH November 2015.
- Staff Development Program on FULL CUSTOM IC DESIGN &FPGA DESIGN FLOW at VNRVJIET, held on February 2012.
- Staff Development Program on DSP PROCESSOR ARCHITECTURES AND PROGRAMMING at VNRVJIET, held on February 2012.

Achievement

- Successfully completed IUCEE EPICS DESIGN THINKING COURSE.
- Presented a paper in National Conference on Advanced Innovations in Engineering Technology and Management (AIETM-2014) at JBREC and got first prize.
- Got second position in M.TECH project in VLSI system design (ECE).
- Secured 95 percentile in GATE-2011.
- Got gold medal for obtaining the 300 out of 300 marks in Intermediate Mathematics subject.
- Participated in Mathematics quiz and got first prize.
- Got school first in SSC.

Books Published:

None

Research Projects Undertaken:

None