KG REDDY College of Engineering & Technology

DEPARTMENT

OF

ELECTRONICS AND COMMUNICATION ENGINEERING

NAME OF THE LABORATORY	**:**	**ANALOG AND DIGITAL COMMUNICATIONS LAB**
YEAR AND SEM	**:**	**II B.TECH II SEM**
REGULATION/LAB CODE	**:**	**R18/ EC406PC**

ANALOG AND DIGITAL COMMUNICATIONS LABORATORY MANUAL

HOD **PRINCIPAL**

KG REDDY College of Engineering & Technology

DEPARTMENT VISION

To be recognized as a full-fledged center for learning and research in various fields of Electronics and Communication Engineering through industrial collaboration and to provide consultancy for solving the real time socio-economic problems.

DEPARTMENT MISSION

- To provide innovative teaching and learning in the contemporary technologies in Electronics and Communication Engineering to support the professional aspirations of the students.
- To promote innovation through research and development among faculty and students by providing opportunities for inter-disciplinary learning in collaboration with industry.
- To encourage professional development of students that will inculcate ethical values and leadership skills while working with the community to address societal issues.

KG REDDY College of Engineering & Technology

Program Outcomes(PO's):

A graduate of the Electronics and Communication Engineering Program will demonstrate:

PO1: **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2: **Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6: **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: **Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one"s own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: **Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Educational Objectives (PEO's):

- **PEO 1:** To be equipped with skills for solving complex real-world problems related to VLSI, Embedded Systems, Signal/Image processing, and Digital and Wireless Communication.
- **PEO 2:** To develop professional skills that will equip them to succeed in their careers and encourage lifelong learning in advanced areas of Electronics and communications and related fields.
- **PEO 3:** To communicate effectively, work collaboratively and exhibit high levels of professionalism, moral and ethical responsibility.
- **PEO 4:** To develop the ability to understand and analyze engineering issues in a broader perspective with ethical responsibility towards sustainable development.

Program Specific Outcomes(PSO's)

- **PSO 1: Problem Solving Skills –** Graduates will be able to apply their knowledge in emerging electronics and communication engineering techniques to design solutions and solve complex engineering problems.
- **PSO 2: Professional Skills –** Graduate will be able to think critically, communicate effectively, and collaborate in teams through participation in co and extra-curricular activities.
- **PSO 3: Successful Career –** Graduates will possess a solid foundation in Electronics and Communications engineering that will enable them to grow in their profession and pursue lifelong learning through post-graduation and professional development.
- **PSO 4: Society Impact –** Graduate will be able to work with the community and collaborate to develop technological solutions that would promote sustainable development in the society.

SYLLABUS

R18 B.TECH ECE

EC406PC ANALOG AND DIGITAL COMMUNICATIONS LAB

B.Tech. II Year II Sem. **L T P C**
0 0 3 1.5

Note:

- Minimum 12 experiments should be conducted
- All these experiments are to be simulated first either using MATLAB, COMSIM or any other simulation package and then to be realized in hardware

List of Experiments:

1. (i) Amplitude modulation and demodulation (ii) Spectrum analysis of AM

2. (i) Frequency modulation and demodulation (ii) Spectrum analysis of FM

3. DSB-SC Modulator & Detector

4. SSB-SC Modulator & Detector (Phase Shift Method)

5. Frequency Division Multiplexing & De multiplexing

6. Pulse Amplitude Modulation & Demodulation

7. Pulse Width Modulation & Demodulation

8. Pulse Position Modulation & Demodulation

9. PCM Generation and Detection

10. Delta Modulation

11. Frequency Shift Keying: Generation and Detection

12. Binary Phase Shift Keying: Generation and Detection

13. Generation and Detection (i) DPSK (ii) QPSK

COURSE OUTCOMES:

CO1. The fundamentals of basic communication system, types of noise affecting communication system and noise parameters.

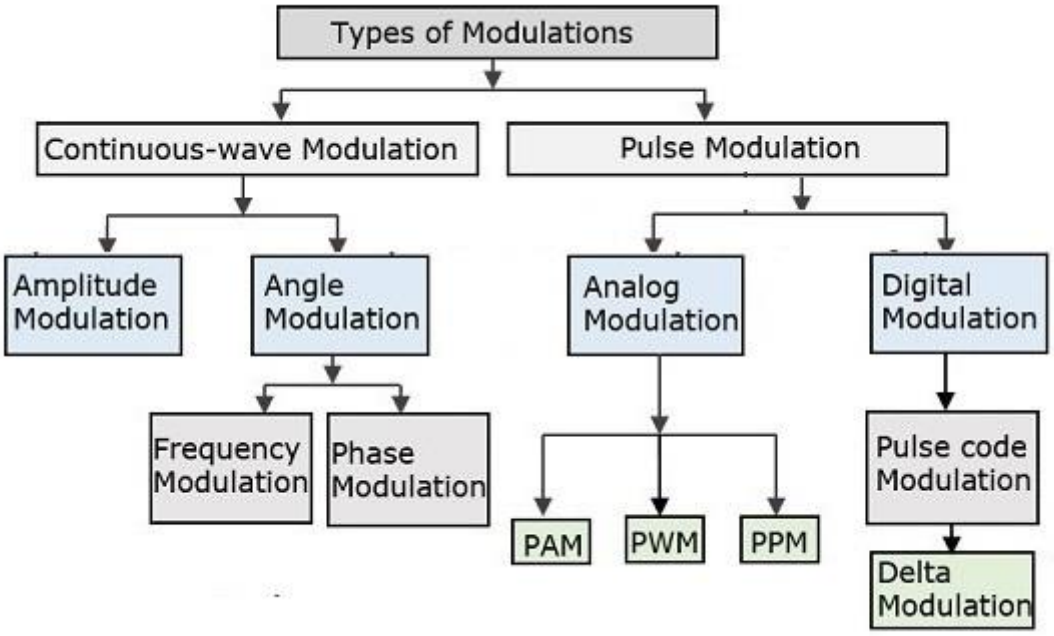
CO2. Need of modulation, modulation processes and different amplitude modulation schemes

CO3. Different angle modulation schemes with different generation and detection methods.

CO4. Learn about theoretical bounds on the rates of digital communication system and represent a digital signal using several modulation methods

CO5. Draw signal space diagrams compute spectra of modulated signals and apply redundancy for reliable communication.

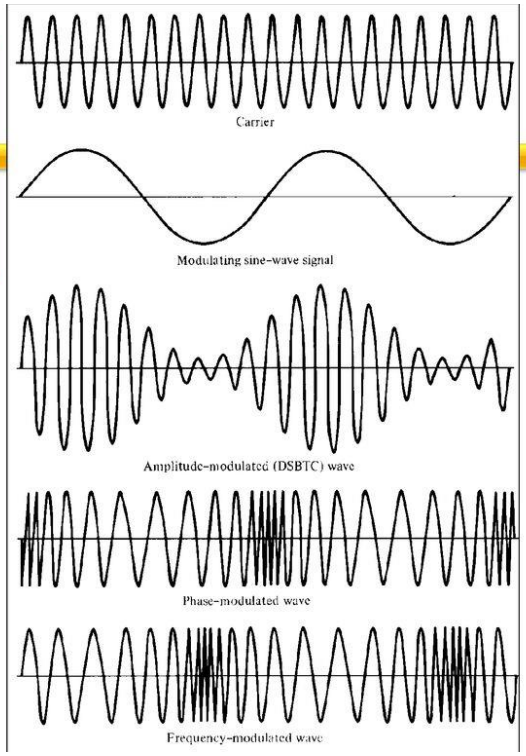
Analog and Digital Communications Introduction:

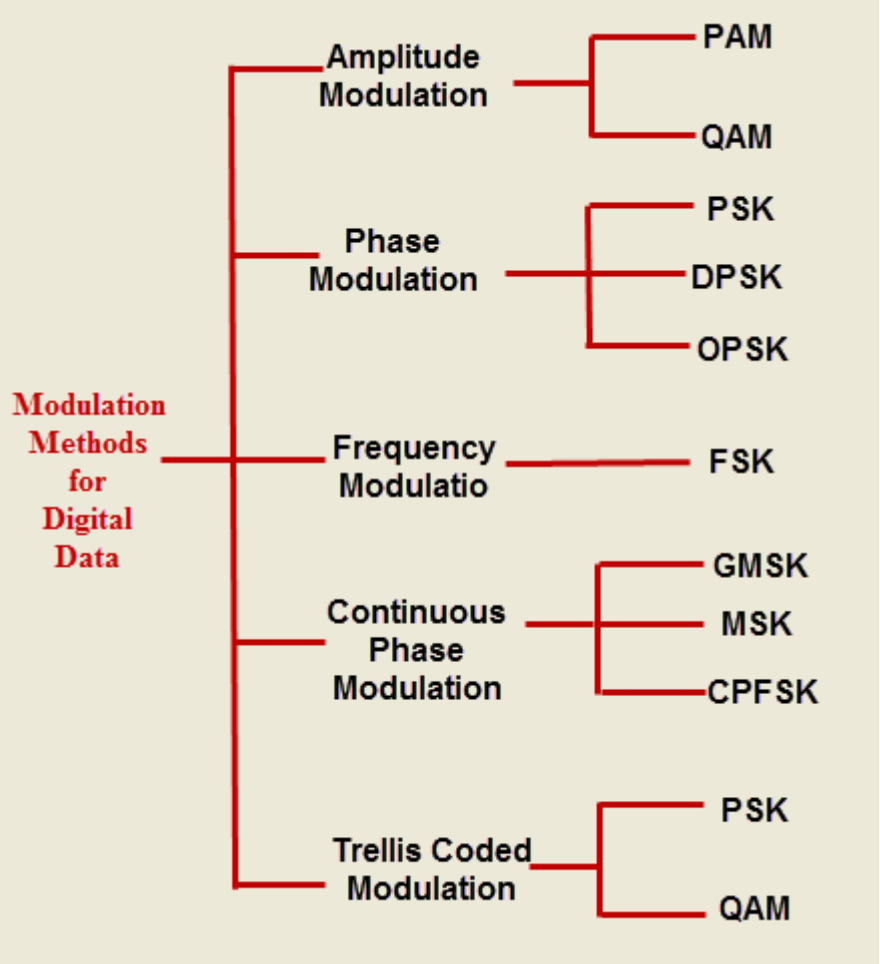


Analog Modulation Techniques

1. Amplitude Modulation (AM)
2. Frequency Modulation (FM)
3. Phase Modulation (PM).

- AM is the simplest form of modulation
- both FM and PM require greater bandwidth than AM.




Modulation Methods for Digital Data
Amplitude Modulation
PAM
QAM
Phase Modulation
PSK
DPSK
OPSK
Frequency Modulatio
FSK
Continuous Phase Modulation
GMSK
MSK
CPFSK
Trellis Coded Modulation
PSK
QAM

DIGITAL COMMUNICATION SYSTEMS

1. Pulse Amplitude Modulation & Demodulation.
2. PWM Modulator & Demodulator.
3. PPM Modulator & Demodulator.
4. 2 Channel TDM (PAM).
5. Sampling Theorem Verification.
6. Pulse Code Modulation & Demodulation.
7. Differential Pulse Code Modulation & Demodulation.
8. Frequency Shift Keying and Demodulation.
9. Phase Shift Keying (PSK).
10. Differential Phase Shift Keying.
11. Delta Modulation and Demodulation.

Features of all Trainers:

- All the trainers are designed as per the syllabus of various universities in India.
- Approved by well-experienced professors from many leading engineering colleges.
- Onboard signal generators and regulated power supplies.
- Wired circuitry of actual circuit.
- All inputs, outputs and test points are terminated with 2mm socket for reliable contact.
- Glass epoxy printed circuit board is used for long life.
- Compact powder coated metal box for rugged use.
- Only test equipments (like Oscilloscope, DMM etc.) are required to conduct specified experiment.
- Regulated power supply ±12V
- Wired circuitry for Common Emitter amplifier

Pulse Amplitude Modulation & Demodulation:

A trainer for demonstration of Pulse Amplitude Modulation (PAM) & Demodulation of PAM signal. This kit consists of

1. Regulated power supply ±12V.
2. Wired circuitry for PAM Modulator using IC 4052.
3. Onboard AF generator.
4. Onboard Pulse generator.
5. Onboard reconstructing network.

Pulse Width Modulation & Demodulation:

A trainer kit to demonstrate PWM operation. This kit consists of

1. Control signal generator.
2. AF signal generator.
3. DC source.
4. PWM modulator.
5. PWM demodulator.
6. Regulator Power Supply ±5V.

FUNCTION GENERATOR

Function generator is a very useful & versatile laboratory instrument. It can be used to test or service any audio devices, like microphones, loud-speakers, pickups, amplifiers. It can also be used as a tone generator & to modulate RF signals. The instrument is very useful to conduct student's projects and to design test simple sub-systems in laboratories. New improved design features gives reliable working even in adverse environments. The versatile bench top unit is useful in R&D, education, industry, and service applications.

Features:

- Digital meter for frequency reading.
- TTL output.
- Fine variable output controls for frequency & amplitude.
- This equipment is compact and easy to maintain.
- Extremely useful in electronics laboratory in designing and testing of new circuits and conducting project experiments for students.
- Less in weight.

Specifications:

Power	:	230V AC $\pm$10%, 50Hz.
Frequency range	:	1Hz to 1MHz in 6 Ranges.
Function	:	Sine, Square, Triangle & TTL output.
Output amplitude	:	0-20 V_{PP} for sine, triangle; 0-15 V_{PP} for square.
Output impedance	:	600 ohms typical on x1 mode; 50 ohms typical on x0.1 mode.
DC offset	:	$\pm$10V with adjustable to 0V.
Output coupling	:	DC coupling.
Frequency accuracy	:	1Hz to 100KHz at $\pm$1% FSD; 100KHz to 1MHz at $\pm$2% FSD.
Size	:	90(H), 255(W), 220(D) all in mm.
Weight	:	3Kg approximately.

Contents:

SOFTWARE PROGRAMS

CONTENTS

EXPERIMENT: 1
AMPLITUDE MODULATION AND DEMODULATION (II) SPECTRUM ANALYSIS OF AM

AIM:

To study the Circuit of AM Modulation & Demodulation

APPARATUS REQUIRED:

- AM modulator trainer kit (FT1501)
- Set of 2mm patch chords - 8 No's
- User Manual.
- CRO
- CRO probes
- Connecting wires
- Adaptor

THEORY:

In Amplitude modulation, the amplitude of a carrier signal is varied by the modulating voltage whose frequency is invariably lower than that of the carrier frequency. In practice, the carrier frequency may be high − frequency (HF), while the modulating frequency is audio frequency, Formally, AM is defined as a system of modulation in which the amplitude of the carrier signal is made proportional to the instantaneous amplitude of the modulating voltage.

Let the carrier voltage and the modulating voltage, Vc and Vm respectively be represented by

$$Vc(t) = Vc \sin wct \quad Vm(t) = Vm \sin wmt$$

Note that phase angle has been ignored in both expressions since it is unchanged by the amplitude modulation process. Its inclusion here would merely complicate the preceding without affecting the result. However, it will certainly not be possible to ignore phase angle when we deal with frequency and phase modulation.

From the definition of AM, it follows that the maximum amplitude Vc of the un modulated carrier will have to be made proportional to the instantaneous modulating voltage Vm Sin wmt when the carrier is amplitude modulated.

BLOCK DIAGRAM:

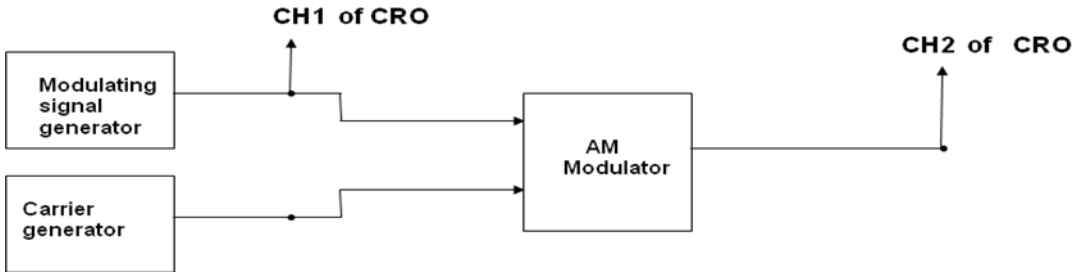


Figure: AM modulator

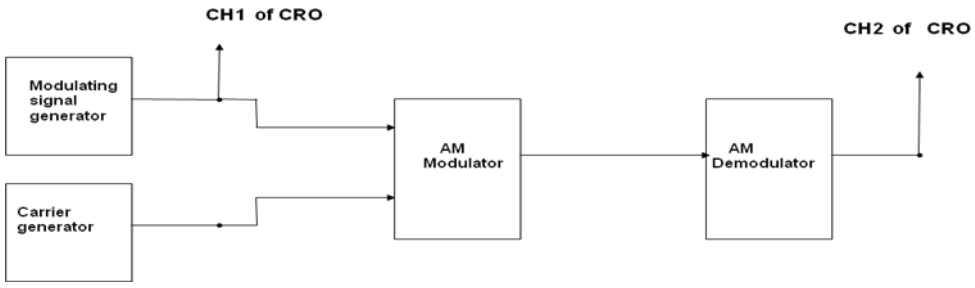


Figure: AM Demodulator

Amplitude Modulation is defined as a process in which the amplitude of the carrier wave c(t) is varied linearly with the instantaneous amplitude of the message signal m(t).The standard form of an amplitude modulated (AM) wave is defined by

$S(t) = Ac\,[1 + Kam(t)] \cos(2\pi fct)$

Where *Ka* is a constant called the amplitude sensitivity of the modulator.

The demodulation circuit is used to recover the message signal from the incoming AM wave at the receiver. An envelope detector is a simple and yet highly effective device that is well suited for the

demodulation of AM wave, for which the percentage modulation is less than 100%. Ideally, an envelop detector produces an output signal that follows the envelop of the input signal wave form exactly; hence, the name. Some version of this circuit is used in almost all commercial AM radio receivers.

The Modulation Index is defined

$$m = \frac{Emax - Emin}{Emax + Emin}$$

Where Emax and Emin are the maximum and minimum amplitudes of the modulated wave.

CIRCUIT DIAGRAMS:

For modulation:

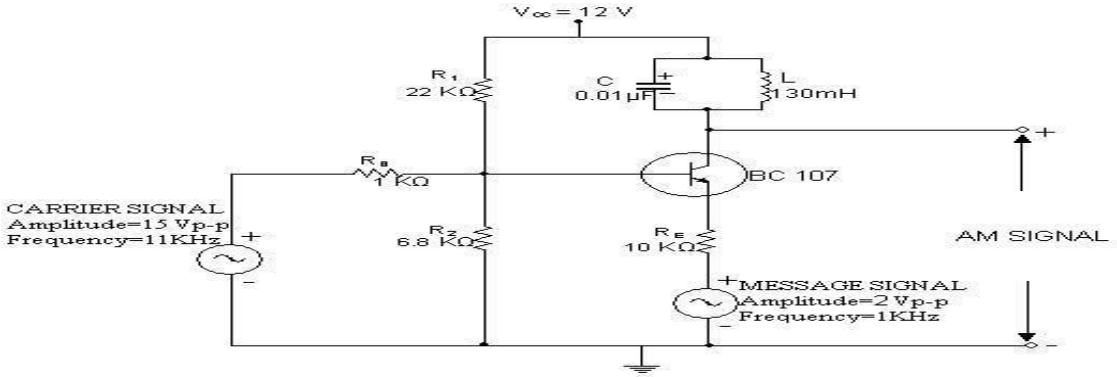


Fig. AM modulator

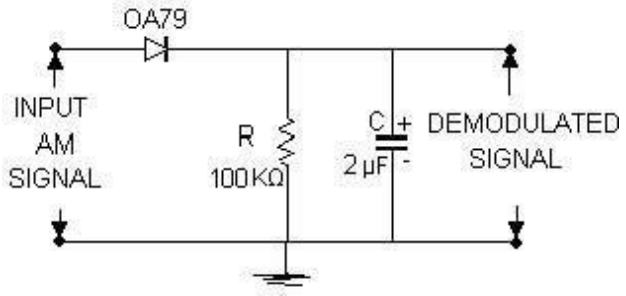
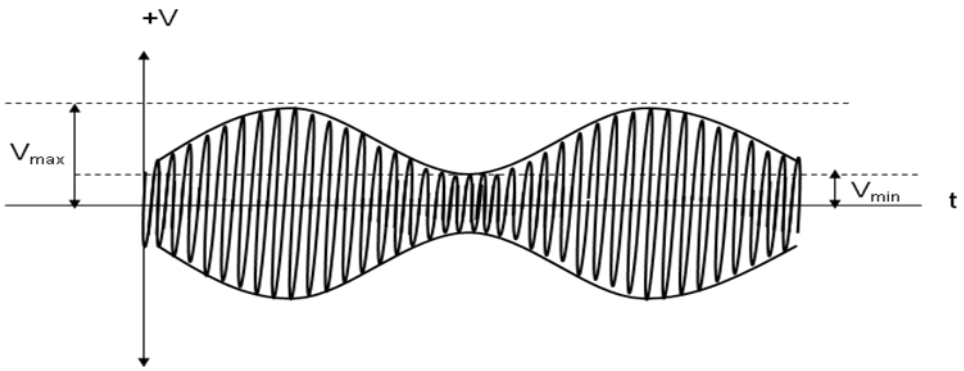


Fig.. AM demodulator

EXPERIMENTAL PROCEDURE:

1. Connect the AC Adaptor to the mains and the other side to the experiential trainer Switch ON the power
2. Observe the carrier and modulating waveforms and note their frequencies.

3. Carrier frequency is around 100 KHZ amplitude is variable from 0-8vp-p Modulating signal is 1KHZ (Approx.).
4. Connect the carrier and modulating signals to the modulator circuit.
5. Observe the amplitude modulating signals to the modulated wave in synchronization with the modulating signal on a dual trace CRO following fig shows the connections.
6. Connect carrier I/p to ground and apply a 2v peak to peak AF signal to carrier I/P to (modulating I/P) and adjust P1 for extreme anti clock wise position to get minimum AC O/P
7. Connect modulating I/p to ground and apply a 3v peak to peak AF signal to carrier I/P and adjust P2 for extreme anti clock wise position to get minimum AC O/P
8. Connect modulating I/P &carrier I/P to ground and adjust P3 for zero DC O/P Make modulating I/P 2vp-p and carrier I/P 3vp-p and adjust P4 for maximum O/P. calculate maximum and minimum points on the modulated envelope on a CRO and calculate depth of modulation from the waveform



9. Observe that varying the modulating voltage, the depth of modulation varies.
10. During demodulation connect this AM O/P to the I/P of the demodulator
11. By adjusting the RC time constant (i.e. cut off frequency) of the filter circuit we get minimum distorted O/P
12. Observe that this demodulated O/P is amplified has some phase delay because of RC components
13. Also observe the effects by changing the carrier amplitudes.
14. In all cases, calculate the modulation index with the help of the following table.

OBSERVATIONS:

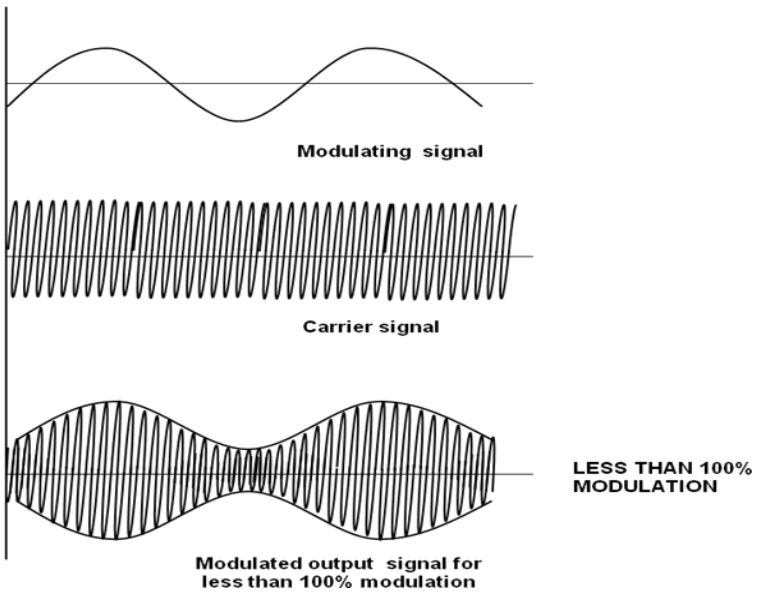
modulating signal: amplitude, frequency

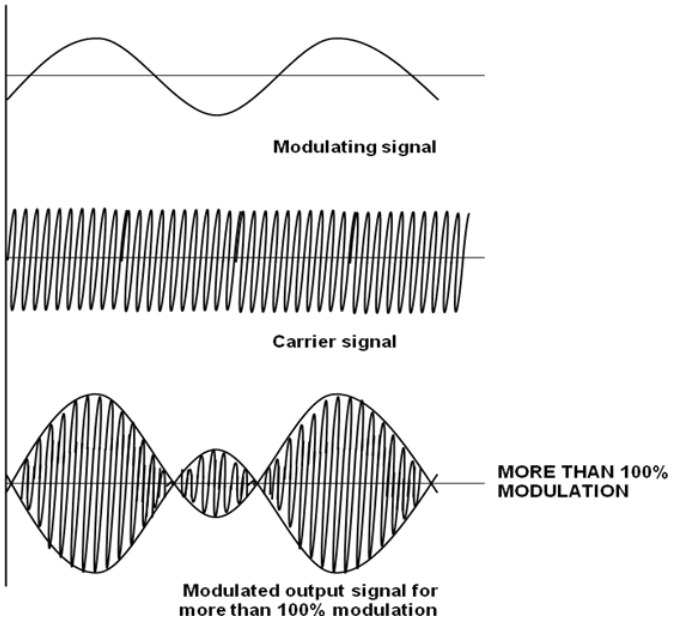
carrier signal: amplitude, frequency

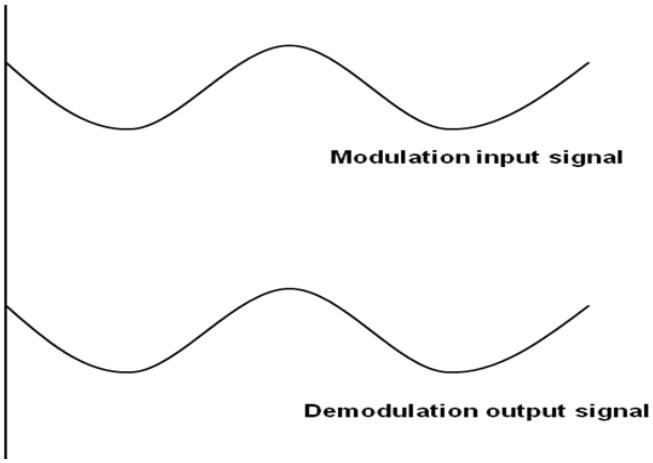
TABULAR FORM:

S. NO:	Am	Ac	Vmax	Vmin	modulation index
1					
2					
3					
4					
5					
6					
7					

WAVEFORMS AND GRAPHS







RESULT:

VIVA QUESTIONS

1. Define AM and draw its spectrum?
2. Draw the phase's representation of an amplitude modulated wave?
3. Give the significance of modulation index?
4. What are the different degrees of modulation?
5. What are the limitations of square law modulator?

EXPERIMENT:2
FREQUENCY MODULATION AND DEMODULATION (II) SPECTRUM ANALYSIS OF FM

AIM

To study the process of Frequency Modulation and Demodulation and to calculate the depth of modulation by varying the modulating voltage.

APPARATUS REQUIRED:

- FM Modulation and Demodulation trainer kit
- CRO probes
- Connecting wires
- Adaptor

THEORY

Frequency modulation is a system in which the amplitude of the modulated carrier is kept constant, while its frequency is varied by the modulating signal. The first practical system was put forward in 1936 as an alternative to AM in an effort to make radio transmissions more resistant to noise. Phase Modulation is a similar system in which the phase of the carrier signal is varied instead of its frequency; as in FM, the amplitude of the carrier signal remains constant. The general equation of an unmodulated wave, or carrier wave may be written as,

$$x = A \sin (wt + q)$$

where x = instantaneous value of voltage or current of carrier.

A = (maximum) amplitude

w = angular velocity; radians per second (rad/s) q = Phase angle (radians)

Note that we represent an angle in radians.

If any one of these three parameters is varied in accordance with another signal, normally of a lower frequency, then the second signal is called the modulation and the first is said to be modulated by the second. In the frequency modulation, frequency of the carrier is made to vary. For simplicity, it is again assumed that the modulation signal is sinusoidal. This signal has two important parameters which must be represented by the modulation process without distortion namely, its amplitude and frequency. It is assumed that the phase relations of a complex modulation signal will be preserved. By the definition of frequency modulation, the amount by which the carrier frequency is varied from its unmodulated value, called the deviation, which is made proportional to the instantaneous value of the modulating voltage. The rate at which this frequency variations or oscillations takes place is naturally equal to the modulating frequency.

The situation is illustrated in Fig − 1, which shows the modulating voltage and the resulting frequency − modulated wave. Fig − 1 also shows the frequency variation with time which is seen to be identical to the variation with time of the modulating voltage. As an example of FM, all signals having the same amplitude will deviate the carrier frequency by the same amount, say 45 KHz, no matter what their frequencies are, similarly all signals of the same frequency say 2 KHz, will deviate the carrier at the same rate of 2000 times per second, no matter what their individual amplitudes are. The amplitude of the frequency modulated wave remains constant at all times. This is infact, the greatest single advantage of FM.

MATHEMATICAL REPRESENTATION OF FM

The instantaneous frequency of the frequency modulated wave is given by $f = fc (1+ K V_m \cos w_m t)$

where fc = unmodulated (or average) carrier frequency K = proportionally constant

$V_m \cos w_m t$ = instantaneous modulating voltage (cosine being preferred for simplicity in calculations)

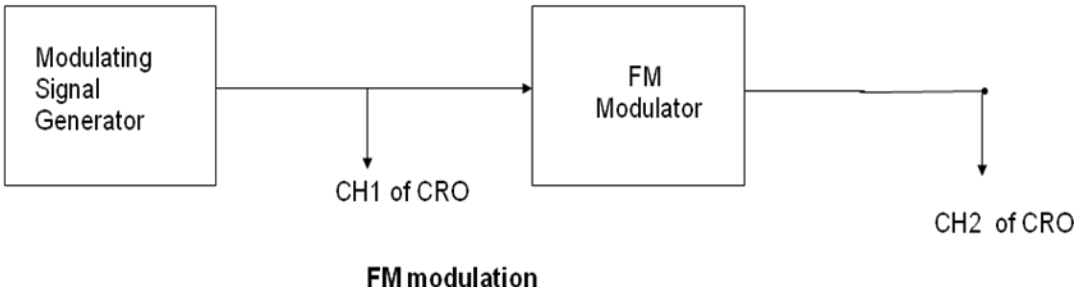
The modulation index for FM, mf is defined as,

$$mf = \frac{\text{max. frequency deviation}}{d} \text{ modulating frequency}$$

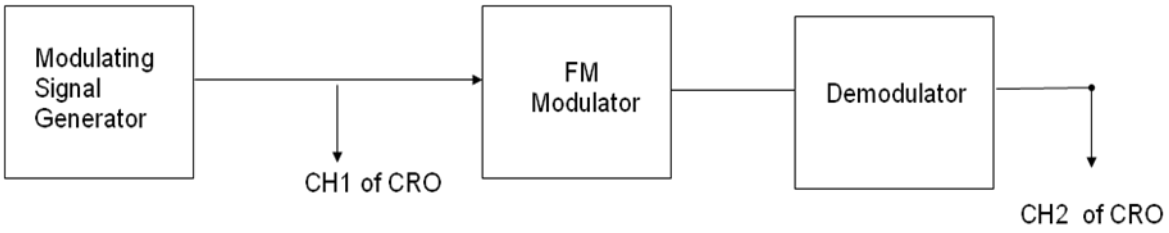
$$= \frac{}{} fm$$

$$V = A \sin (w_c t + mf \sin w_m t)$$

BLOCK DIAGRAM:



FM modulation



FM Demodulation

EXPERIMENTAL PROCEDURE

1. Connect the AC Adaptor to the mains and the other side to the Experimental Trainer.
2. Observe carrier signal and modulating signals on a dual trace CRO.
   a. Carrier signal: Modulator output without any modulating input. Carrier frequency is 100 KHz and amplitude of 5Vp − p.
   b. Modulating signal: Frequency is 10KHz.
   Amplitude is 5V p − p. (Variable)
3. Connect modulating signal to the modulator input and observe modulating signal and FM output on a dual trace CRO.
4. Trigger CRO w.r.t. CH1. Adjust amplitude of the modulating signal until we get undistorted FM output. It is difficult to trigger FM on analog CRO. That is why you adjust modulating signal amplitude until small distortion notified in FM output.
5. Calculate maximum frequency and minimum frequency from the FM output and calculate modulating index.
6. During demodulation connect the circuit as shown below.
7. Adjust the potentiometer in demodulation section until we get demodulated output.

OBSERVATIONS AND CALCULATIONS:

Modulating signal: amplitude (Am):
Frequency (fm):
Carrier signal: amplitude (Ac): Frequency (fc):

Band width:

The Band Width required for FM signal, as per Carson's rule is Band Width B = 2 (Δf + fm)
Band width is twice the sum of frequency deviation and the modulating frequency The modulation index β = $\frac{\Delta f}{fm}$

When Δ f = frequency deviation fm = modulating frequency

TABULAR FORM:

S. NO:	**Am**	**fmax**	**frequency deviation=**Δ f fmax-fc	**modulation index** β =	**Band Width**BW = 2 (Δf + fm)
1					
2					
3					
4					

WAVEFORMS:

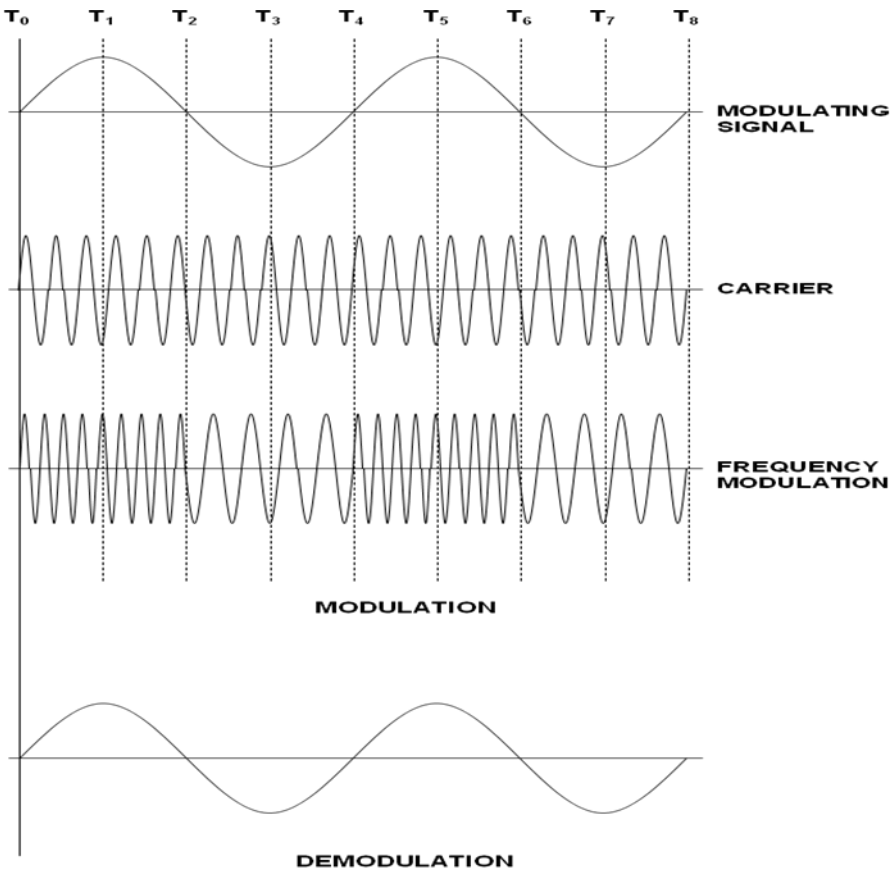


Fig – 3 Modulations and Demodulation

RESULT:

VIVA QUESTIONS:

1. Define FM & PM.
2. What are the advantages of Angle modulation over amplitude modulation?
3. What is the relationship between PM and FM?
4. With a neat block diagram explain how PM is generated using FM.

EXPERIMENT: 3
DSB-SC MODULATOR & DETECTOR

AIM

To study the working of DSB Balanced modulatior & Sync detector.

APPARATUS REQUIRED

- DSB-SC Modulation and Demodulation trainer kit
- CRO probes
- Connecting wires
- Adaptor

THEORY

INTRODUCTION

DSB BALANCED MODULATIOR & SYNC DETECTOR is an useful educational kit for the demonstration of Balanced Modulator. After completion of this experiment you will be

1. Understand frequency doubling using balanced modulator
2. Double side Band suppressed carrier modulation

DESCRIPTION

1. CARRIER SIGNAL GENERATOR

This is a sine co-sine generator using OP-AMP. IC TL 084 is used as an active component. TL 084 is a FET input general purpose quad OP-AMP integrated circuit. An individual controls are provided to vary the output voltage. It is generating fixed 100KHz frequency with 00 and 900 phases.

2. MODULATING SIGNAL GENERATOR

This is a sine co-sine generator using OP-AMP. IC TL 084 is used as an active component, TL 084 is a FET input general purpose quad OP-AMP integrated circuit. An individual controls are provided to vary the output voltage. It is generating fixed 3KHz frequency with 00 and 900 phases.

3. MODULATOR

This has been developed using MC 1496 IC. MC 1496 is a monolithic integrated circuit Balanced Modulator/Demodulator, is versatile and can be used up to 200MHz. These modulators are used in this experiment to produce DSB-SC signals. Controls is provided to balance the output. This trainer contains balanced Modular of 2 no.s. They are Balanced Modulator (A), Balanced Modulator (B).

4. DEMODULATOR

The base band signal m(t) can be uniquely recovered from a DSB-SC signal s(t) by first multiplying s(t) with a locally generated sine wave carrier and then low pass filtering the

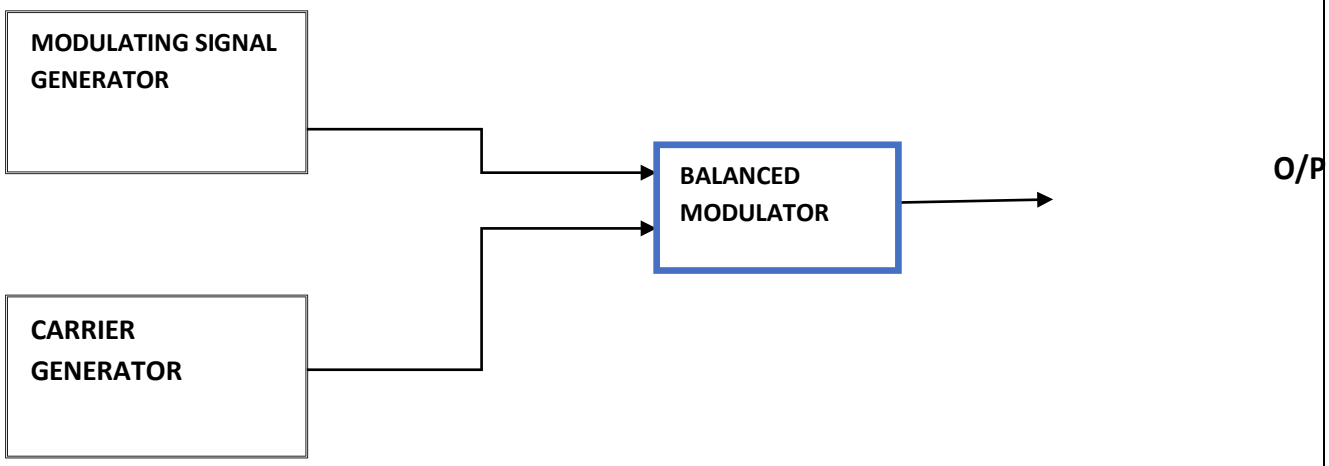
product. It is assumed that the local oscillator signal is exactly coherent or synchronous, in both frequency and phase with the carrier wave c(t) used in the balanced modulator to generate s(t). This method of demodulation is known as coherent detection or synchronous detection.

In this unit IC MC 1496 is used as synchronous demodulator. The MC 1496 is a monolithic balanced modulator/ balanced demodulator, is versatile and can be used up to 200MHz. On board generated carrier (which is used in the modulator) is used as synchronous signal.

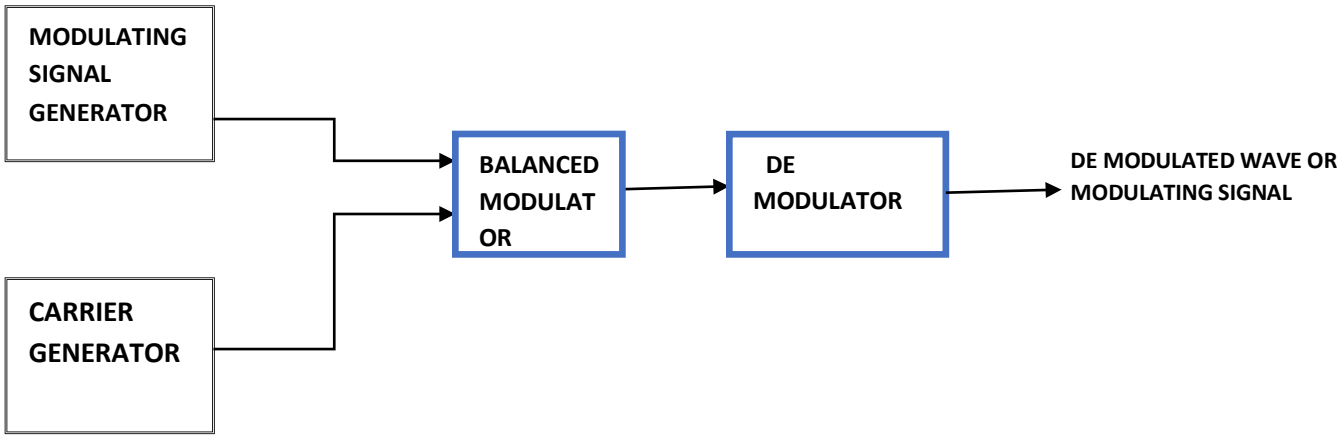
6. REGULATED POWER SUPPLY

This consists of bridge rectifier, capacitor filters and three terminal fixed voltage regulators (7812,7912,7908) to provide required DC voltage in the circuit I.e. ±12v and -8v @ 150mA each.

BLOCK DIGRAM MODULATOR



DE MODULATOR



CIRCUIT DIAGRAM

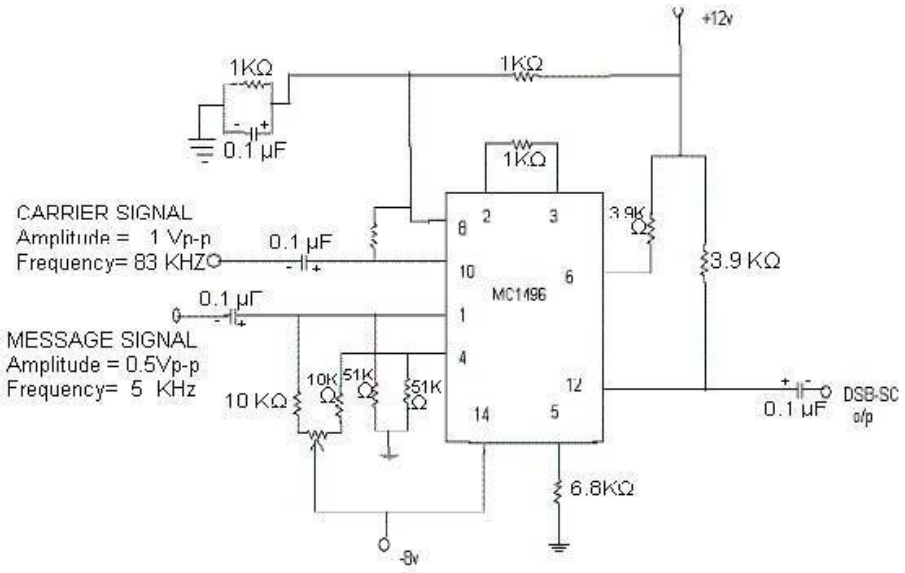


Fig. Balanced Modulator Circuit

EXPERIMENTAL PROCEDURE:

1. As the circuitry is already wired you just have to trace the circuit according to the circuit diagram given above.
2. Connect the AC Adaptor to the mains and the other side to the experiential trainer. Switch ON the power.

3. Measure the output voltage of regulated power supply circuit.
4. Connect same 5KHZ sinusoidal signal (note that inputs of 0.1 to 0.4 appear to be acceptable but if there is distortion re reduce the amplitude) to both the carrier and modulation I/Ps.
5. Observe the O/P on an oscilloscope and adjust the carrier null potentiometer (the one provided in modulator block) until the O/P is a 10 KHZ sinusoidal. Nate that this is a very sensitive adjustment because you are making the basing at both I/P exactly the same to get the multiplying effect of the device, check the input and O/P frequencies using a frequency counter and verify that you have exact multiplication by 2 in frequency
6. Change the input frequency and verify that you have multiplication at 1000KHZ and 500KHZ.note that there is a decrease in amplitude at the higher frequencies but multiplying action continues.

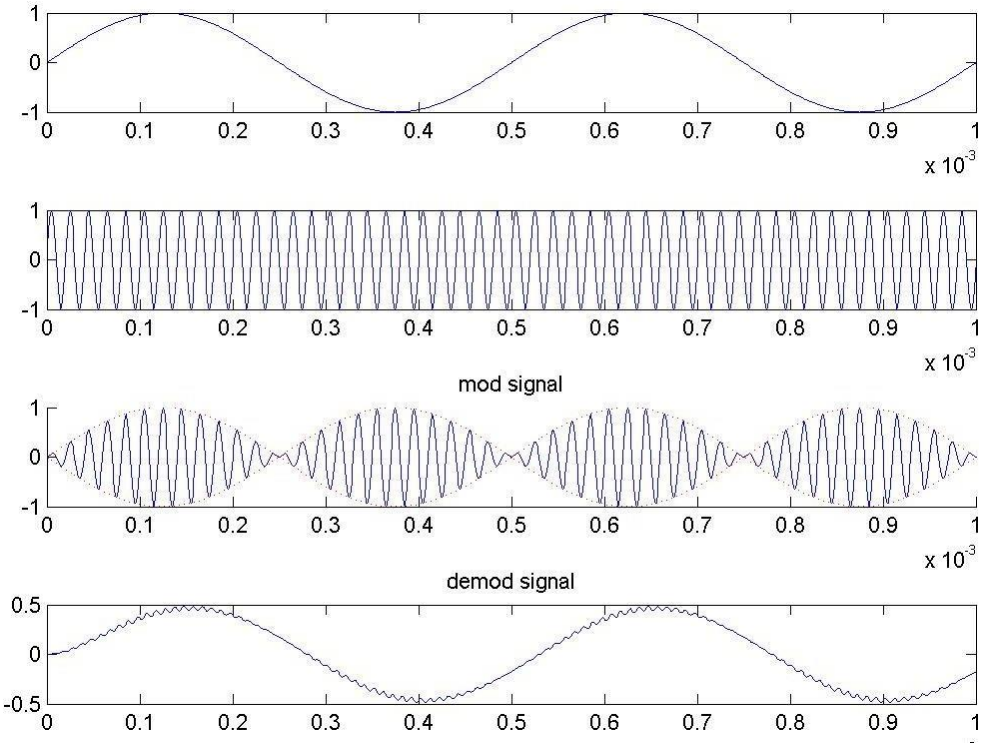
AM DSB /SC

1. Apply a 1000KHZ, 0.1 peaks sinusoidal to the carrier input and a 5 kHz, 0.1 peaks sinusoidal to the modulation input.
2. Adjust the carrier null potentiometer to obtain a wave form like the one in figure if spectrum analyzer is available observe and sketch the output in the frequency domain

SAMPLE READINGS:

Signal	AMPLITUDE (Volts)	Frequency (Hz)
Message signal	0.5V	5 KHz
Carrier signal	1V	83.3KHz
DSB-SC Signal	1.92V p-p	

WAVEFORM S:



PRECAUTIONS:

1. Check the connections before giving the supply
2. Observations should be done carefully

OBSERVATIONS:

Phase reversal in DSB-SC Signal is occur at the zero crossing of modulating signal.

RESULT:

VIVA QUESTIONS:

1. What are the two ways of generating DSB_SC?
2. What are the applications of balanced modulator?
3. What are the advantages of suppressing the carrier?
4. What are the advantages of balanced modulator?
5. What are the advantages of Ring modulator?

EXPERIMENT: 4

SSB-SC MODULATOR & DETECTOR (PHASE SHIFT METHOD)

AIM:

To generate the SSB modulated wave.

APPARATUS REQUIRED:

- SSB-SC Modulation and Demodulation trainer kit
- CRO probes
- Connecting wires
- Adaptor

THEORY:

An SSB signal is produced by passing the DSB signal through a highly selective band pass filter. This filter selects either the upper or the lower sideband. Hence transmission bandwidth can be cut by half if one sideband is entirely suppressed. This leads to single-sideband modulation (SSB). In SSB modulation bandwidth saving is accompanied by a considerable increase in equipment complexity.

BLOCK DIAGRAM:

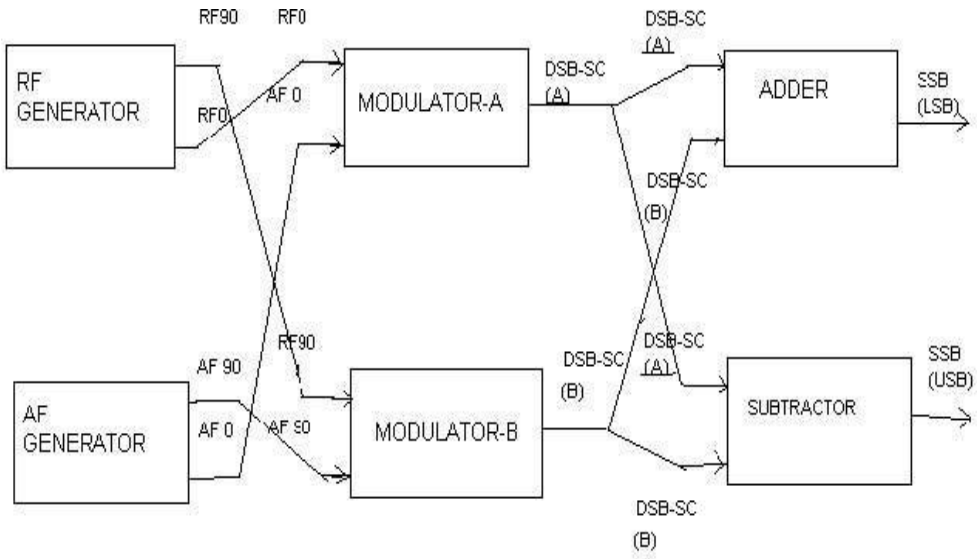


Fig. Single Side Band system

EXPERIMENTAL PROCEDURE GENERATION OF UPPER SIDE BAND (SSB)

Connect the AC Adaptor to the mains and the other side to the Experimental Trainer. Switch 'ON' the power.

1. a) connect carrier fc 900 to A in of Balanced Modulator - A and adjust its amplitude to 0.1Vpp
   b) Connect modulating signal fm 00, 5Vpp to Bin of the Balanced Modulator-A.
2. Observe the DSB-A output on a spectrum analyzer. Both the side bands fc+ fm (100KHz + 5KHz) and fc - fm (100KHz - 5KHz) are seen on the screen. Measure the respective power levels in dB also.
3. Connect fc 00 at 0.1Vpp at Cin of Balanced Modulator B. Connect fm 900 at 5Vpp at Din of Balanced Modulator B.
4. Observe the spectrum at DSB-B output which again gives the side bands fc + fm & fc - fm
5. Connect the DSB-A output and DSB-B output to the summing amplifier. Observe the output (SSB output) on the spectrum analyzer. This gives single side band (upper) only while the lower side band is cancelled in the summing Amplifier.

II. GENERATION OF LOWER SIDE BAND SPECTRUM

1. Repeat the steps mentioned above except that at Cin connect fc 900 to Balanced Modulator B.
2. Observe the spectrum of DSB-A and DSB-B outputs which gives double side bands at fc + fm and fc - fm.
3. Observe the output at 'SSB output' on spectrum analyzer. It gives single side Band (LSB). Thus by phase shift method both LSB or USB can be generated selectively. This method avoids the complete filters required to suppress the unwanted side Band.

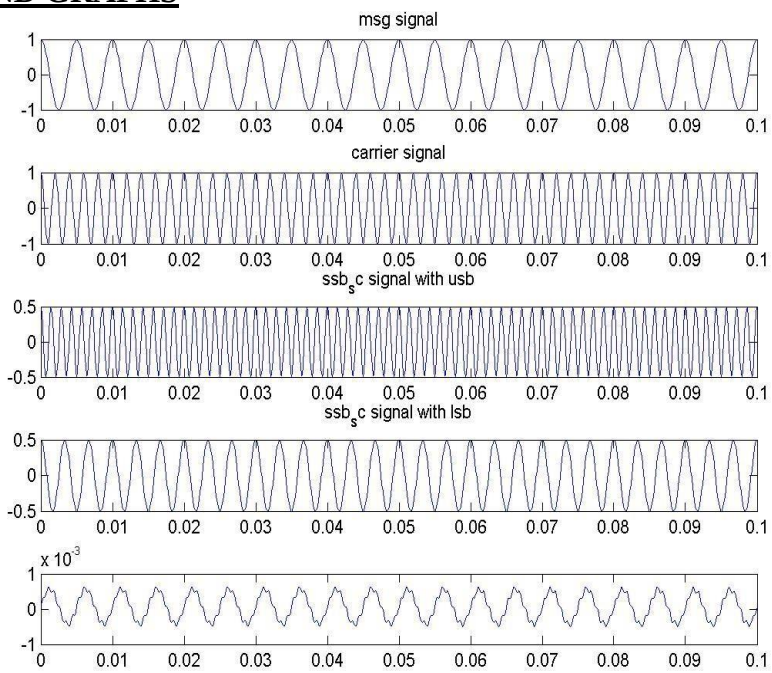
DEMODULATOR

1. Connect the carrier fc 00 and SSB output to the synchronous detector.
2. Observe the demodulator output on the oscilloscope which is the recovered modulating signal.

SAMPLE READINGS

Signal	Amplitude (volts)	Frequency (KHz)
Message signal	2	1
Carrier signal	2	100
SSB (LSB)	0.5	98.54
SSB (USB)	0.42	101.4

WAVEFORMS AND GRAPHS



RESULT:

VIVA QUESTIONS:

1. What is single side band system.
2. How many methods are there to generate the SSB
3. What are the advantages to transmit the single side band.

EXPERIMENT NO-5
FREQUENCY DIVISION MULTIPLEXING& DE MULTIPLEXING

AIM: To study the frequency division multiplexing and De Multiplexing Techniques.

APPARATUS/SOFTWARE REQUIRED:

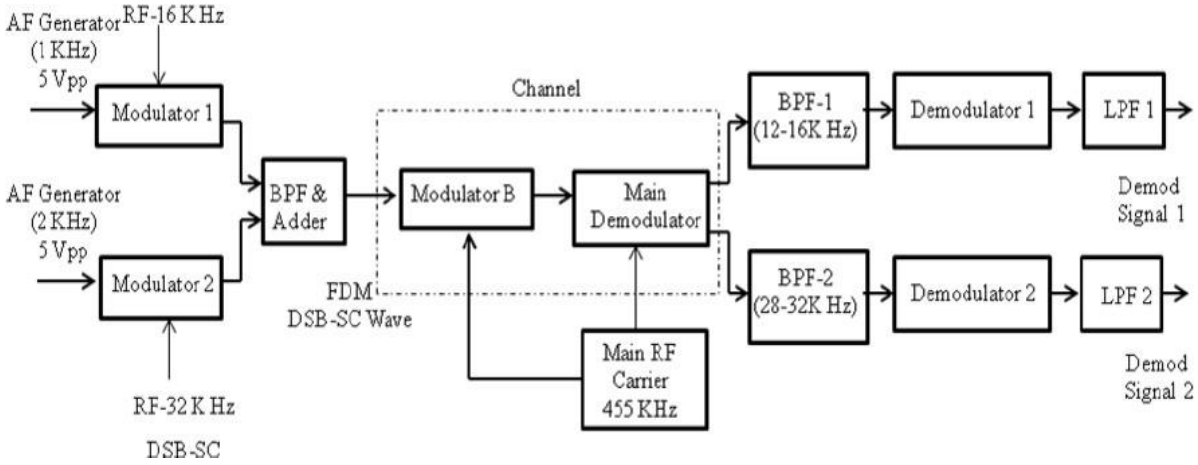
1. FREQUENCY DIVISION MULTIPLEXING & DEMULTIPLEXING Trainer Kit.
2. C.R.O (30 MHz)
3. Patch chords.

THEORY:

In Frequency Division Multiplexing, Data Streams are carried simultaneously on the same Transmission medium by allocating to each of them a different Frequency Band within the Bandwidth of the Single Channel.

Multiplexing is done by equipment called Multiplexer (MUX). It is placed at the Transmitting End of the communication link. At the Receiving End, the Composite Signal is separated by equipment called Demultiplexer (DEMUX). Demultiplexer performs the reverse process of Multiplexing and routes the separated signals to their corresponding Receivers or Destinations.

BLOCK DIAGRAM:



EXPERIMENTAL PROCEDURE:

FDM Multiplexing:

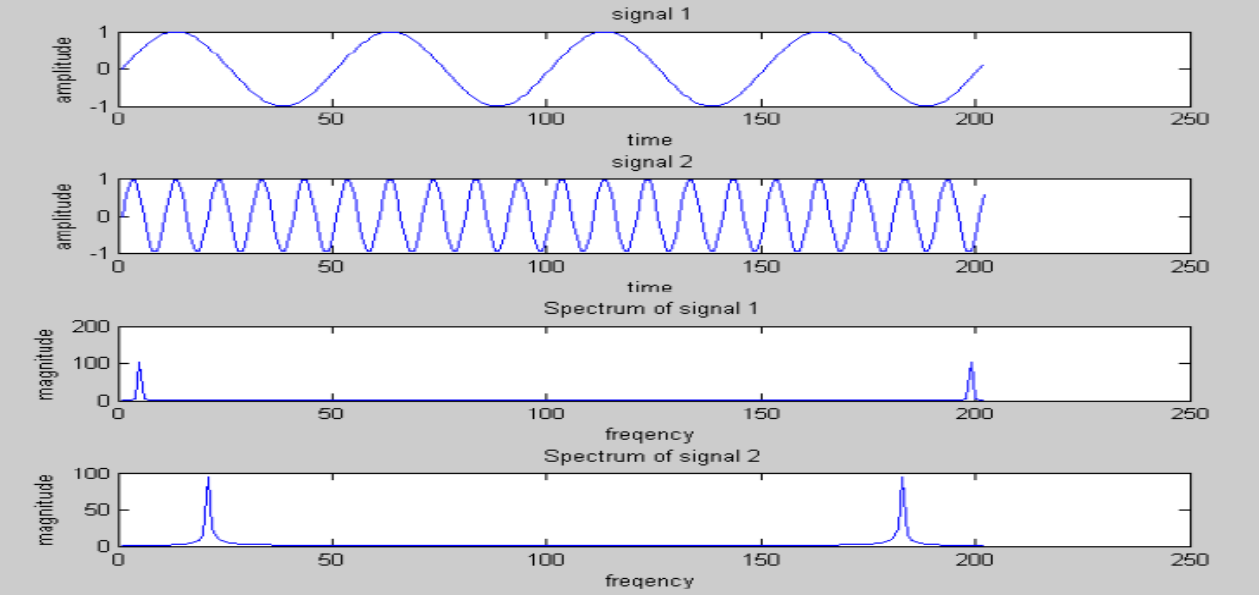
1. Connect the circuit as shown in the figure.
2. Switch ON the power supply.
3. Set the amplitude of each modulating signal as 5Vp-p and frequency ofeach AF signal to 1kHz and 2kHz respectively.
4. Monitor the outputs at Tp1(signal-1), Tp2(signal-2),Tp10(RF-16kHz),Tp12(RF-32KHz),Tpq(modulation-1),Tp11(Modulator-2),Tp17(BPF & adder)

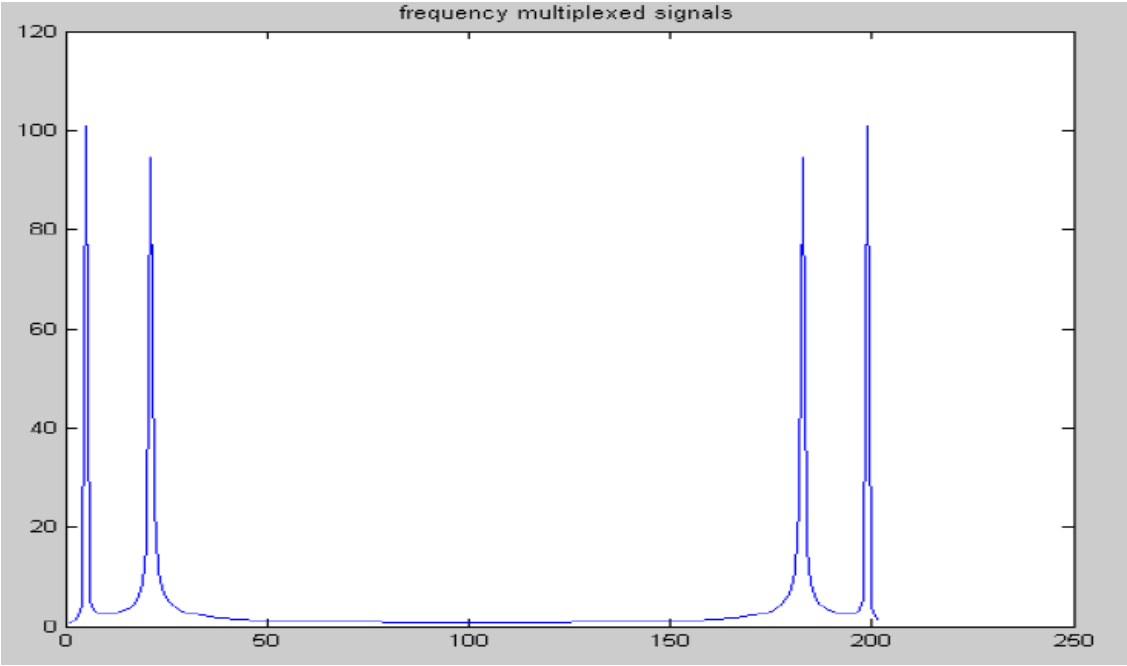
5. Set output frequency of RF oscillator to 455 kHz and amplitude to10Vp-p.
6. Monitor the output at Tp18 the FDM DSB-SC wave will be observed.

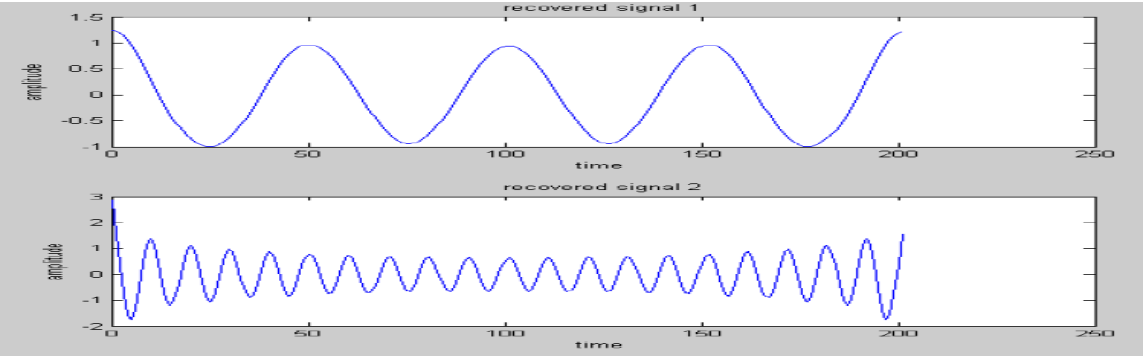
FDM DeMultiplexing & LPF:

1. Connect the Tp18 to Tp22 and observe the output of main demodulator at Tp23.
2. Connect the main demodulator output to the BPF1 (28-32 kHz) and BPF1 (12-16 kHz).
3. Connect the output of BPF, s to the respective demodulator and then to LPF, s.
4. Monitor the demodulated signal1 and at TP32 and demodulated signal2 atTP39.

Expected waveforms:







RESULT:

VIVA QUESTIONS:

1. What is the application of FDM?
2. Explain the block diagram of FDM?
3. Compare TDM and FDM

EXPERIMENT: 6
PULSE AMPLITUDE MODULATION & DEMODULATION

AIM:

To study Pulse Amplitude Modulation & Demodulation Process

APPARATUS REQUIRED:

- PAM Modulation and Demodulation trainer kit
- CRO probes
- Connecting wires
- Adaptor

HARDWARE DESCRIPTION

1. AF Signal Generator 200 Hz to 2 kHz (Frequency and Amplitude variable)
2. Synchronous Clock Generator 8 kHz output and 1 KHz input.
3. PAM Modulator
   a) Natural Sampling
   b) Sample and Hold
   c) Flat - Top Sampling
4. PAM Demodulator consisting of
   Low Pass Filter (3.4 kHz cut off) and Amplifier.
   Built-in power supplies ± 12V/350 mA, ±5V/350 mA.

THEORY OR CIRCUIT DESCRIPTION INTRODUCTION

Pulse Modulation may be used to transmit analog information, such as continuous speech or data. It is a system in which continuous waveforms are sampled at regular intervals. Information regarding the signal is transmitted only at the sampling times, together with any synchronising Pulse that may be required. At the receiving end, the original waveforms may be reconstructed from the information regarding the samples, if these are taken frequently enough. Despite the fact that information about the signal is not supplied continuously, as in Amplitude Modulation and Frequency modulation, the resulting receiver output can have regenerate the analog information signal.

Pulse Modulation may be subdivided broadly into two categories, Analog and Digital. In the former, the indication of sample Amplitude may be continuously variable, while in the later a

ode which indicates the sample amplitude to the nearest predetermined level is sent. Pulse Amplitude modulation is a form of analog communication which is discussed in the following section.

PULSE AMPLITUDE MODULATION

In this we have a train of fixed width of pulses. The amplitude of each pulse is made proportional to the amplitude of the modulating signal at that instant. Pulse Amplitude Modulation generation circuit is shown in Fig-5 (Panel layout diagram). Synchronous clock is applied to the base of the

Transistor. Modulating signal (unipolar positive) is given to the collector of the transistor. The output of the transistor (collector current) varies in accordance with the amplitude of the modulating signal voltage resulting in Modulated output.

PULSE AMPLITUDE DEMODULATION

The Demodulation of the Pulse Amplitude Modulation is quite a simple process. Pulse Amplitude Modulated signal is fed to a Low pass Filter, from which the Demodulating signal emerges, whose amplitude at any time is proportional to the pulse amplitude modulation at that time. This signal is given to an inverting amplifier to amplify its level. The demodulated output is almost equal to amplitude with the modulating signal but is phase shifted due to the modulation, demodulation process.

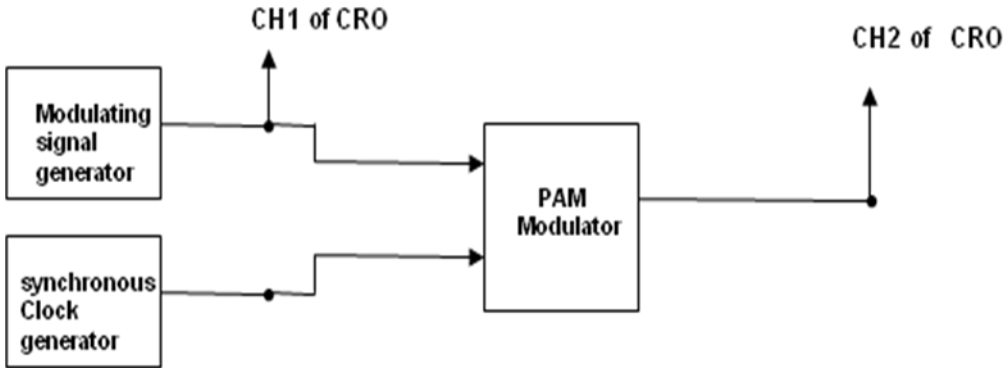


Fig: PAM Modulator

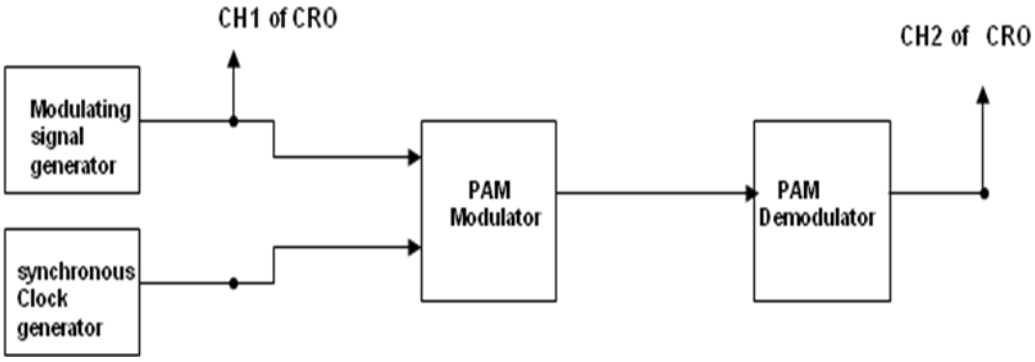


Fig: PAM De Modulator

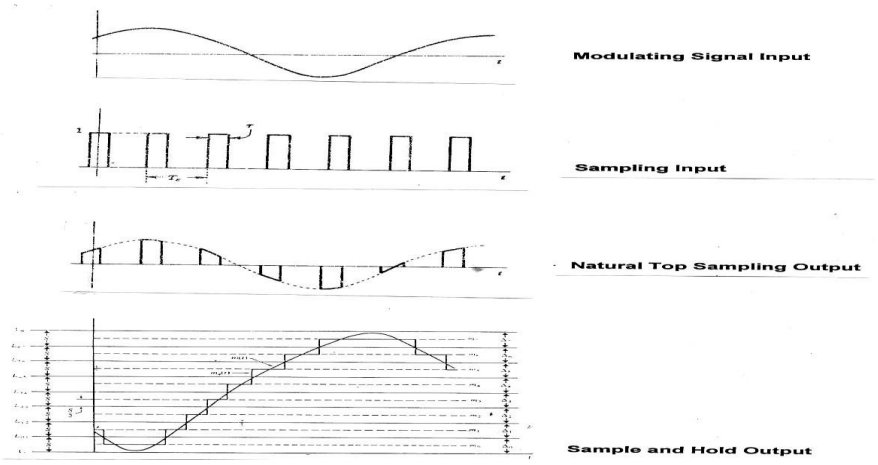
EXPERMIMENTAL PROCEDURE

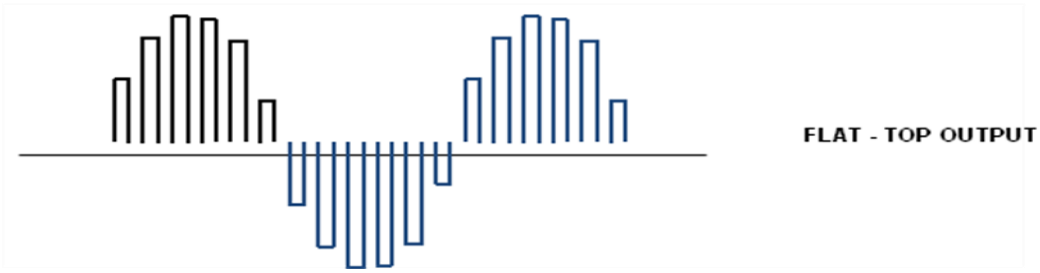
1. Connect the AC Adaptor to the mains and the other side to the Experimental Trainer.
2. Observe the modulating signal and carrier signal (Synchronous clock generator) outputs.
3. Apply the modulating signal generator output and synchronous clock generator output to the PAM modulator.

4. Following Fig. Shows the Testing procedure.
5. By varying the amplitude of the modulating signal, depth of modulation varies.
6. During demodulation, connect PAM output to the input of the PAM demodulator and observe the output of PAM demodulator.

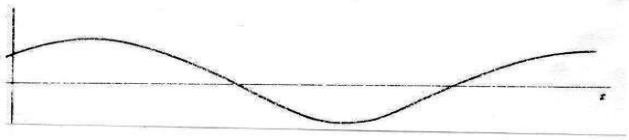
    1. Following Fig. Shows the testing procedure.

EXPECTED WAVEFORMS:





Demodulated Signal



RESULT:

VIVA QUESTIONS:

1. What is cross talk in the context of time division multiplexing?
2. Which is better, natural sampling or flat topped sampling and why?
3. What is the minimum rate at which a speech signal can be sampled for the purpose of PAM?

EXPERIMENT: 07

PULSE WIDTH MODULATION & DEMODULATION

AIM:

To study Pulse Width Modulation & Demodulation Process.

HARDWARE DESCRIPTION

1. AF Signal Generator 200 Hz to 2 kHz (Frequency and Amplitude variable)
2. Synchronous Clock Generator 8 kHz output and 1 KHz input.
3. PWM Modulator
4. PWM Demodulator consisting of
   Low Pass Filter (3.4 kHz cut off) and Amplifier.
   Built-in power supplies ± 12V/350 mA, ±5V/350 mA.

BLOCKDIAGRAM:

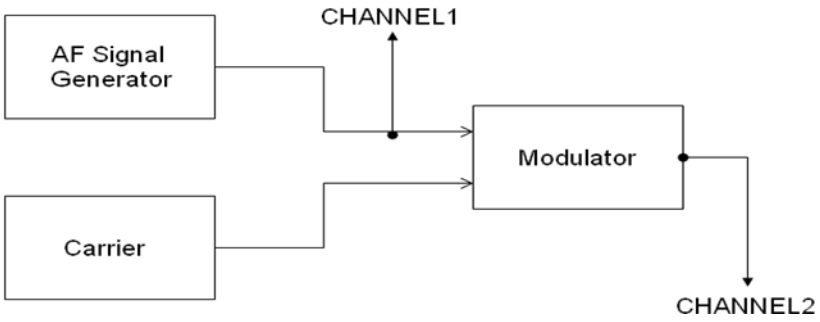


Fig: PWM Modulator

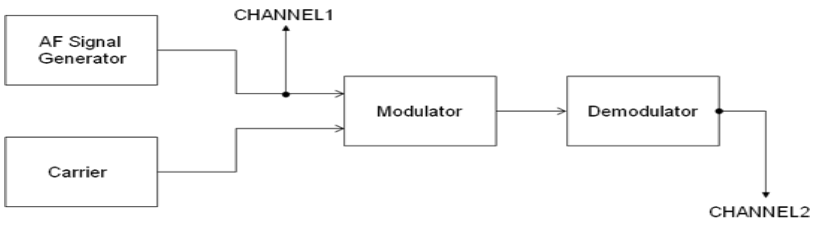
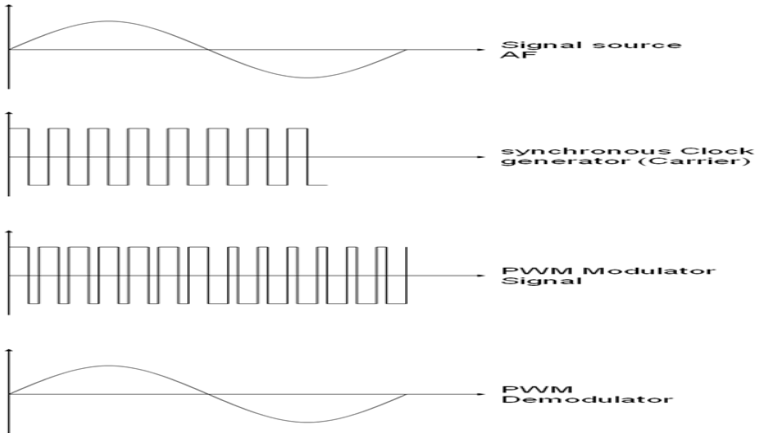


Fig: PWM Demodulator

EXPERIMENTAL PROCEDURE

1. Connect the AC Adaptor to the mains and switch on the Experimental Trainer.
2. Observe the Synchronous clock generator output and AF signal outputs.
3. Connect Synchronous clock generator output to the Synchronous clock input point of PWM modulator and observe the same clock on one channel of a dual trace CRO.
4. A variable amplitude of AF signal is given to observe the PWM output and synchronous clock width varies according to the modulating voltage.
5. Observe the PWM output on CH2 with respect to AF signal on CH1.
6. Trigger the CRO with respect to CH1.
7. During the demodulation apply PWM output signal to the input of demodulator and observe its output on CH2 with respect to CH1 i.e. AF signal.

WAVE FORMS



RESULT:

VIVA QUESTIONS:

1. Why should the curve for pulse width Vs modulating voltage be linear?
2. What is the other name for PWM?
3. What is the disadvantage of PWM?
4. Will PWM work if the synchronization between Tx and Rx fails?

EXPERIMENT:08

PULSE POSITION MODULATION & DEMODULATION

AIM

To study Pulse Position Modulation & Demodulation circuit.

APPARATUS REQUIRED:

- PAM Modulation and Demodulation trainer kit
- CRO probes
- Connecting wires
- Adaptor

THEORY

Pulse Modulation is used to transmit analog information, such as a continuous speech signal. It is a system in which continuous waveforms are sampled at regular intervals. Information regarding the signal is transmitted only at the sampling times, together with any synchronizing pulses that may be required. At the receiving end, the original waveform is reconstructed from the samples, if these are taken frequently enough. Despite the fact that information about the signal is not supplied continuously, as in Amplitude Modulation and Frequency Modulation, the resulting receiver output can have negligible distortion.

Pulse Modulation may be subdivided broadly into two categories, Analog and Digital. In the former, the indication of sample Amplitude may be infinitely variable, while in the latter a code which indicates the sample Amplitude to the nearest predetermined level is sent. Pulse Position Modulation is an analog communication which is discussed in the following section.

PULSE POSITION MODULATION

In Pulse Position Modulation, we have a fixed Amplitude and pulse width of each pulse, but the position of each pulse is made proportional to the Amplitude of the Modulating signal at that instant.

In the PPM Trainer board, Pulse Position Modulation is generated by two Monostable Multivibrators as shown in Panel diagram (PPM Modulator) In this, the first Multivibrator generates the pulse width Modulation output and the second Multivibrator generates the pulse position modulation. Initially, the Synchronous clock from the trainer is given to the pin-2 of the first 555 (IC) (which is connected in Monostable mode) and the AF signal is given to the pin-5 of the same 555 (IC). Now if we observe the output at pin-3 of the same first 555 (IC), we get Pulse Width Modulation signal. The width of each pulse is varied if we change the Amplitude of the AF signal which is applied at pin - 5 of 555(IC).

The output of the 1st 555 (IC) is connected to Pin2 of the 2nd 555 (IC) through a capacitor. So the generated Pulse Width Modulation pulses are used to Trigger the second Monostable Multivibrator. The position of each pulse is varied in accordance with the already generated pulse width modulation. But the PWM depends on the input AF signal. Therefore, the generated pulse position modulation signal depends on the Amplitude of the AF signal. If we change the Amplitude of the AF signal, the position of each pulse is varied. But the width of the each

pulse is remains constant, because the time constant of the second Monostable Multivibrator is constant (fixed).

BLOCK DIAGRAM:

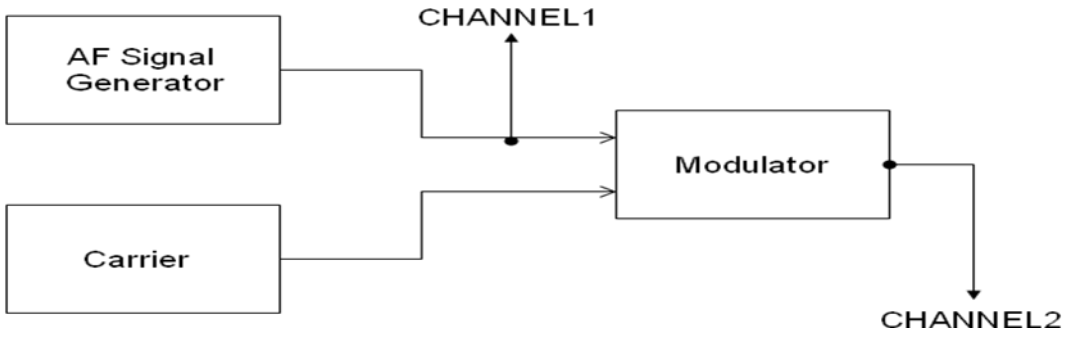


Fig: PPM Modulator

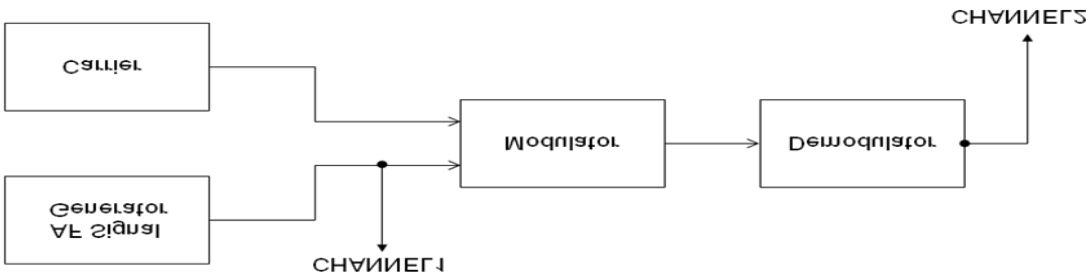
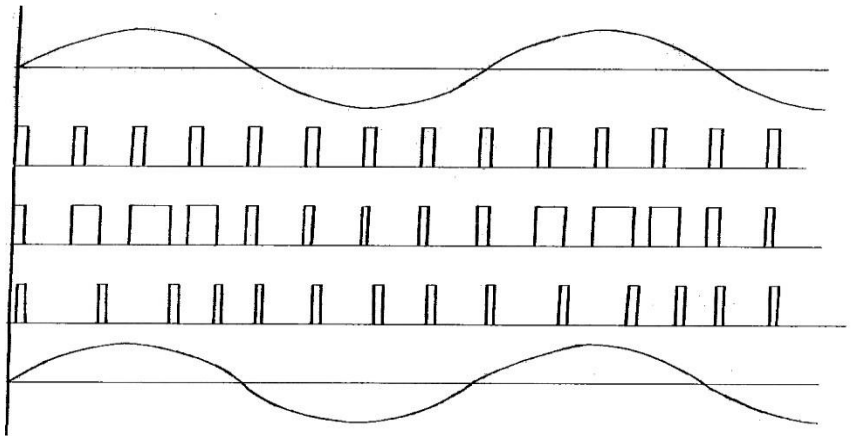


Fig: PPM Demodulator

EXPERIMENTAL PROCEDURE

1. Connect the AC Adaptor to the mains and switch on the Experimental Trainer.
2. Observe the Synchronous clock generator output and AF signal outputs.
3. Connect Synchronous clock generator output to the Synchronous clock input point of PPM modulator and observe the same clock on one channel of a dual trace CRO.
4. A variable amplitude of AF signal is given to observe the PPM output and synchronous clock width varies according to the modulating voltage.
5. Observe the PPM output on CH2 with respect to AF signal on CH1.
6. Trigger the CRO with respect to CH1.
7. During the demodulation apply PWM output signal to the input of demodulator and observe its output on CH2 with respect to CH1 i.e AF signal.

WAVE FORMS:



RESULT

VIVA QUESTIONS:

1. What is the advantage of PPM over PWM?
2. Shift in the position of each pulse of PPM depends on what?
3. Can we generate PWM from PPM?
4. Why do we need 555 timers?
5. Is synchronization critical in PPM?

EXPERIMENT:09

PULSE CODE MODULATION GENERATION AND DETECTION

.**AIM:** To Study Pulse Code Modulation and Demodulation

Equipment and components Required:

S. No	Name of Equipment	Model	Type/Range	Quantity
1	PCM transmitter trainer kit	AET-68M	Dc source:0-5v Freq:200 Hz	1
2	PCM receiver trainer kit	AET-68D		1
3	CRO	Analog	**Freq**:0-20MHz	1
4	Connecting wires	BNC	-	2-3

THEORY: In the PCM communication system, the input analog signal is sampled and these samples are subjected to the operation of quantization. The quantized samples are applied to an encoder. The encoder responds to each such a sample by generation unique and identifiable binary pulse. The combination of quantize and encoder is called analog to digital converter. It accepts analog signal and replaces it with a successive code symbol, each symbol consists of a train of pulses in which the each pulse represents a digit in arithmetic system.

When this digitally encoded signal arrives at the receiver, the first operation to be performed is separation of noise which has been added during transmission along the channel. It is possible because of quantization of the signal for each pulse interval; it has to determine which of many possible values has

been received.

BLOCK DIAGRAM:

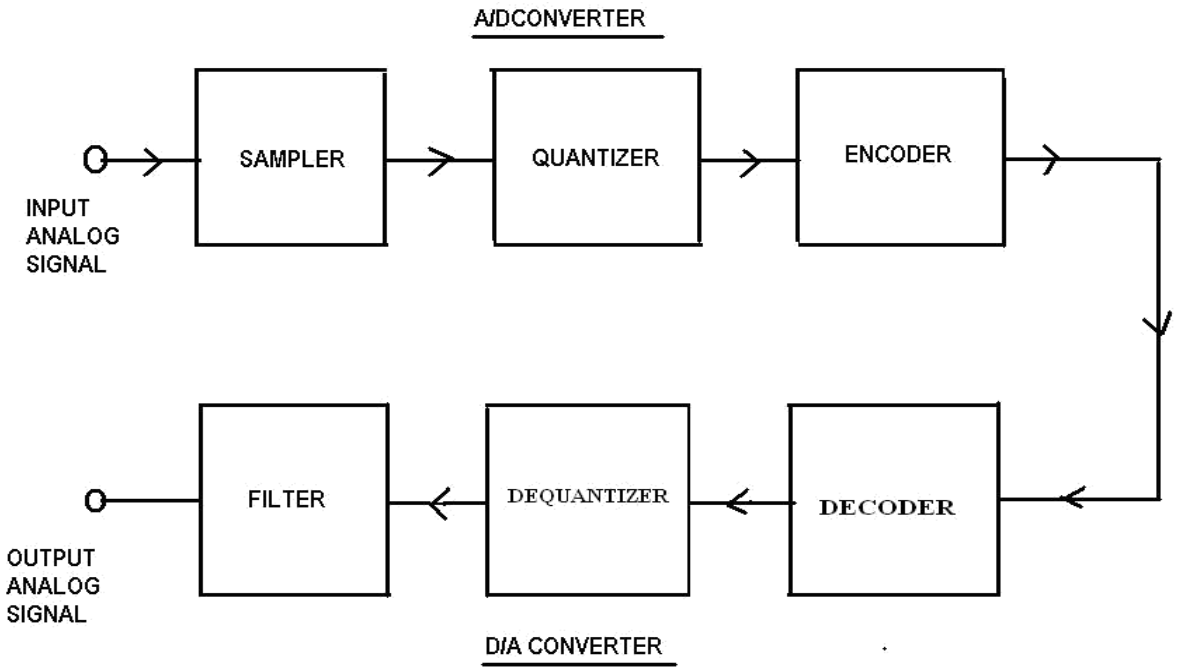


Figure 1 Block diagram of PCM Modulation and Demodulation

OUTPUT WAVEFORM

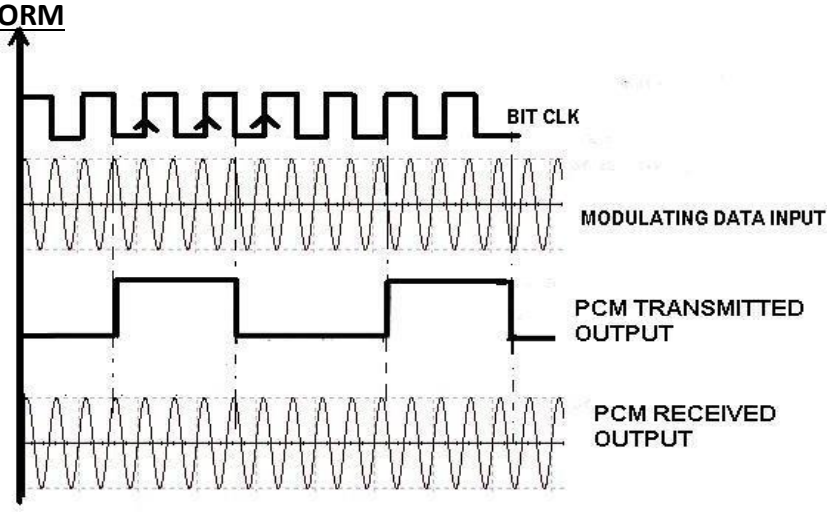


Figure : Output waveform of PCM Modulation and Demodulation

PROCEDURE:

1. The two inputs of function generator are connected to channel -0 and channel-1 simultaneously that is DC_1 output to channel -0 and DC_2 to channel-1.
2. Transmitter and receiver are connected by the synchronization of clock pulses and by connecting ground transmitter to ground receiver.
3. The transmitter is connected to the input of receiver to go the original signal at the receiver output.
4. The phase shift of a channel can be obtained by comparing the input and output of channels at the transmitter block.
5. Thus the output of transmitter can be noted down and input of receiver is similar to that.
6. The receiver output signals are noted down at channel 0 and channel 1 of the receiver block.

RESULT:

Applications:

1. Telecom systems.
2. Digital audio recording.
3. Digitized video effects.
4 . Voice mail.
    1. Radio control units.

Viva questions:

1. What is the expression for transmission bandwidth for PCM?
2. What is the expression for quantization noise/error in PCM?
3. What are the advantages of PCM?
4. What are the disadvantages of PCM?
5. What are the applications of PCM?

Sample questions:

1. What is PCM? Explain PCM modulation and demodulation using block diagram and waveforms.
2. Explain the input and output waveforms of PCM.
3. Explain analogue to digital conversion process in detail using appropriate sketches.
4. What are the advantages and disadvantages of PCM?
5. What are the practical applications of PCM?

EXPERIMENT:10

DELTA MODULATION

AIM: To study the operation of Delta Modulation and Demodulation and observe the waveforms

Equipment Required

S. No	Name of Equipment	Model	Quantity
1	Delta Modulator trainer	AET-73M	1
2	Delta Demodulator trainer	AET-73D	1
3	CRO	Analog	1
4	Multimeter	Digital	1
5	Connecting wires	BNC	2

THEORY: Delta Modulation is almost similar to DPCM. In this only one bit is transmitted per sample just to indicate whether the present sample is larger or smaller than the previous one. The encoding, decoding and quantizing process become extremely simple but this system cannot handle rapidly varying samples. This increases quantizing noise. It has also not found wide acceptance.

BLOCK DIAGRAM FOR MODULATOR

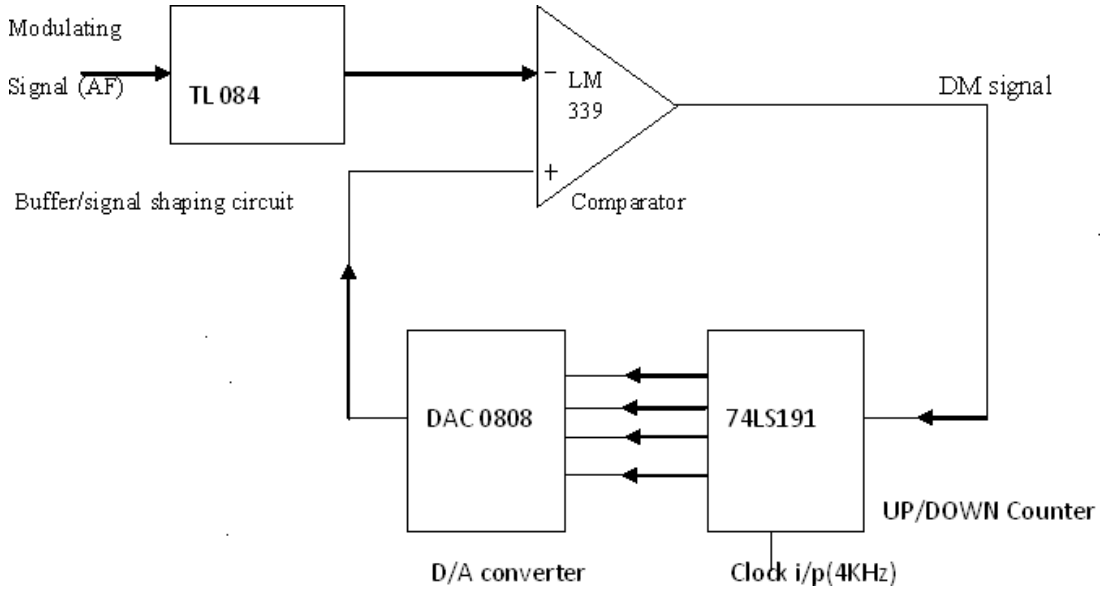


Figure 3. DM MODULATOR

BLOCK DIAGRAM FOR DEMODULATOR:

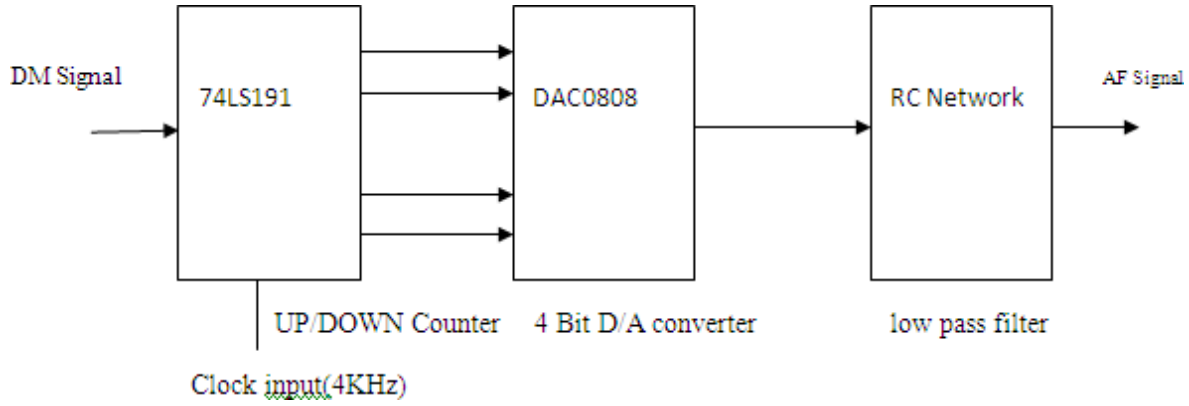


Figure 3.2 Block diagram of Demodulator

PROCEDURE:

MODULATOR

1. 1.Give the 1kHz analog input to the comparator input pin(9) and the output of the comparator is given to the bi-stable circuit input the TX clock signal is given to the other input of the bi-stable circuit.

2. The bi-stable circuit output is internally given to the Unipolar/bipolar converter and the output of this converter will be given to the input of integrator.

3. The integrator output is given to the second input of the comparator.

4. Then plot the comparator input waveforms and the bi-stable circuit output, and the corresponding clock signal.

DEMODULATOR

1. Connect the bi-stable circuit output to the demodulator side bi-stable circuit input, and also give the receiver clock signal to this circuit.

2. The output of this bi-stable circuit is internally given to the Unipolar/bipolar converter and the output of this converter will be given to the input of integrator at demodulator side.

3. Then the integrator output is given to the low pass filter, so finally we observe the original analog signal output across low pass filter output terminal.

OUTPUT WAVEFORMS:

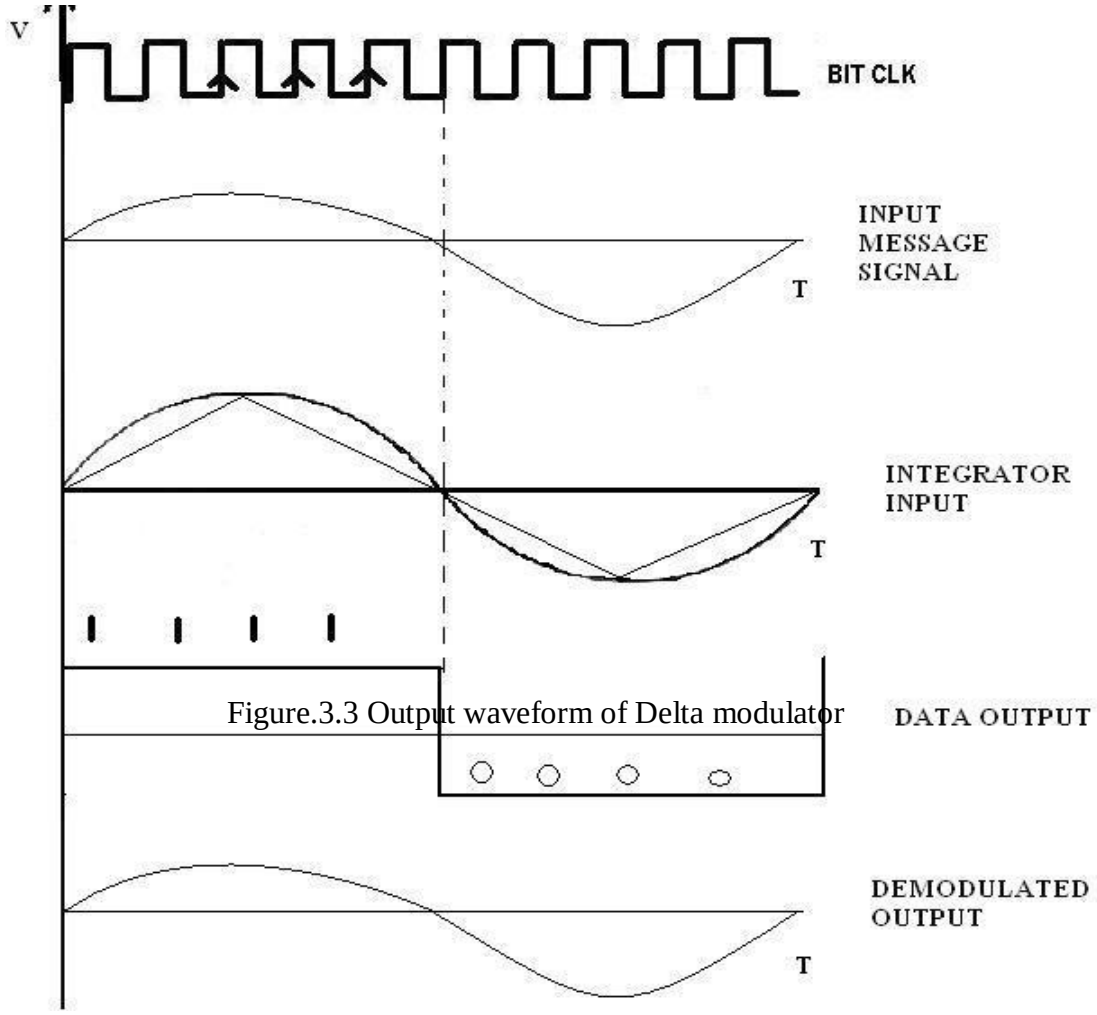


Figure.3.3 Output waveform of Delta modulator

PRECAUTIONS:

1. Connections must be tight.
2. Note down the comparator inputs carefully.

RESULT:

Applications

1. It is used in radio communication devices such as TV remotes. 2It is also used in telecommunications.

Viva voce questions:

1. What are the advantages of Delta modulator?
2. What are the disadvantages of delta modulator?
3. How to overcome slope overload distortion?
4. How to overcome Granular or ideal noise?
5. What are the differences between PCM & DM?
6. Define about slope over load distortion?
7. What is the other name of Granular noise?
8. What is meant by staircase approximation?
9. What are the disadvantages of Delta modulator?
10. Write the equation for error at present sample?

Sample questions:

1. What is Delta Modulation? Explain Delta modulation and demodulation using block diagram and waveforms.
2. Explain the input and output waveforms of Delta Modulation.
3. What are the advantages of Delta Modulation over DPCM?
4. What are the advantages and disadvantages of Delta Modulation?
5. What are the drawbacks of Delta Modulation? How they can be overcome?
6. What are the practical applications of DPCM

EXPERIMENT:11

FREQUENCY SHIFT KEYING: GENERATION AND DETECTION

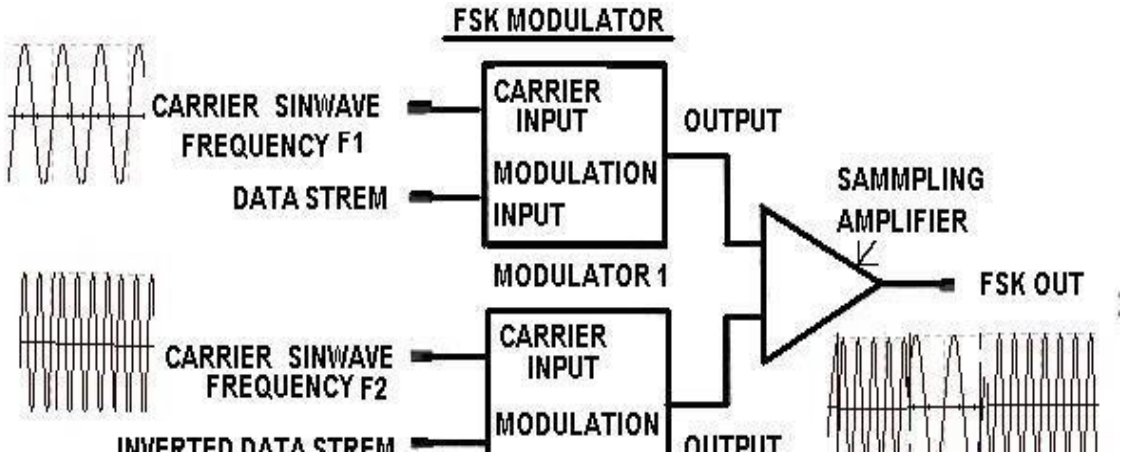
AIM: To study Frequency Shift Keying and observe the waveforms

Equipment Required

S. No	Name of Equipment	Model	Quantity
1	FSK trainer	AET-48	1
2	Dual trace oscilloscope	Analog	1
4	Multimeter	Digital	1
5	Connecting wires	BNC	2

THEORY:

In FSK, the waveform is generated by switching the frequency of the carrier between two values corresponding to the binary information which is to be transmitted. Here the carrier frequency varies from lowest to highest point i.e. carrier swing is known as Frequency shift keying. FSK signaling schemes find a wide range of applications in low speed digital data transmission systems.



BLOCK DIAGRAM

Figure 5.1 Block Diagram of Frequency shift Keying

PROCEDURE; (PCM T_X)

1. D.C 1 to CH.0
    - CH.0 to CH.1
2. The following conditions should be there
    - Mode switch - fast mode
        - Switched faults – OFF
        - Error check code – OFF
        - Adjust D.C1 until the 7 bit code is displayed on A/D converter LED.

(DATA FORMATTING AND CARRIER MOD.&DEMOD. TRAINER)

1. From PCM Tx clock to Tx clock input terminal.
2. PCM output to Tx data input.
3. Then connect NRZ (L) output, carrier of 1.44MHz is applied at modulating input& carrier inputs of Modulator I.
4. Now invert the NRZ (L) output, then the inverted output and 960MHz carrier signal both are given to Modulator II.
5. Both the outputs of Modulator I& Modulator II are given to a summing amplifier then we observe the FSK output across the summing amplifier output terminal.
6. For demodulation of this FSK signal, connect this FSK output to FSK demodulator input terminal and the output of this FSK demodulator block is given to the input of LPF.
7. The LPF output is given to the input of voltage comparator, then we observe the demodulated output across the output terminal of the voltage comparator of DF&CDM trainer kit.

PRECAUTIONS:

1. Connections must be tight.
2. Carefully draw the output waveform

OUTPUT WAVEFORMS

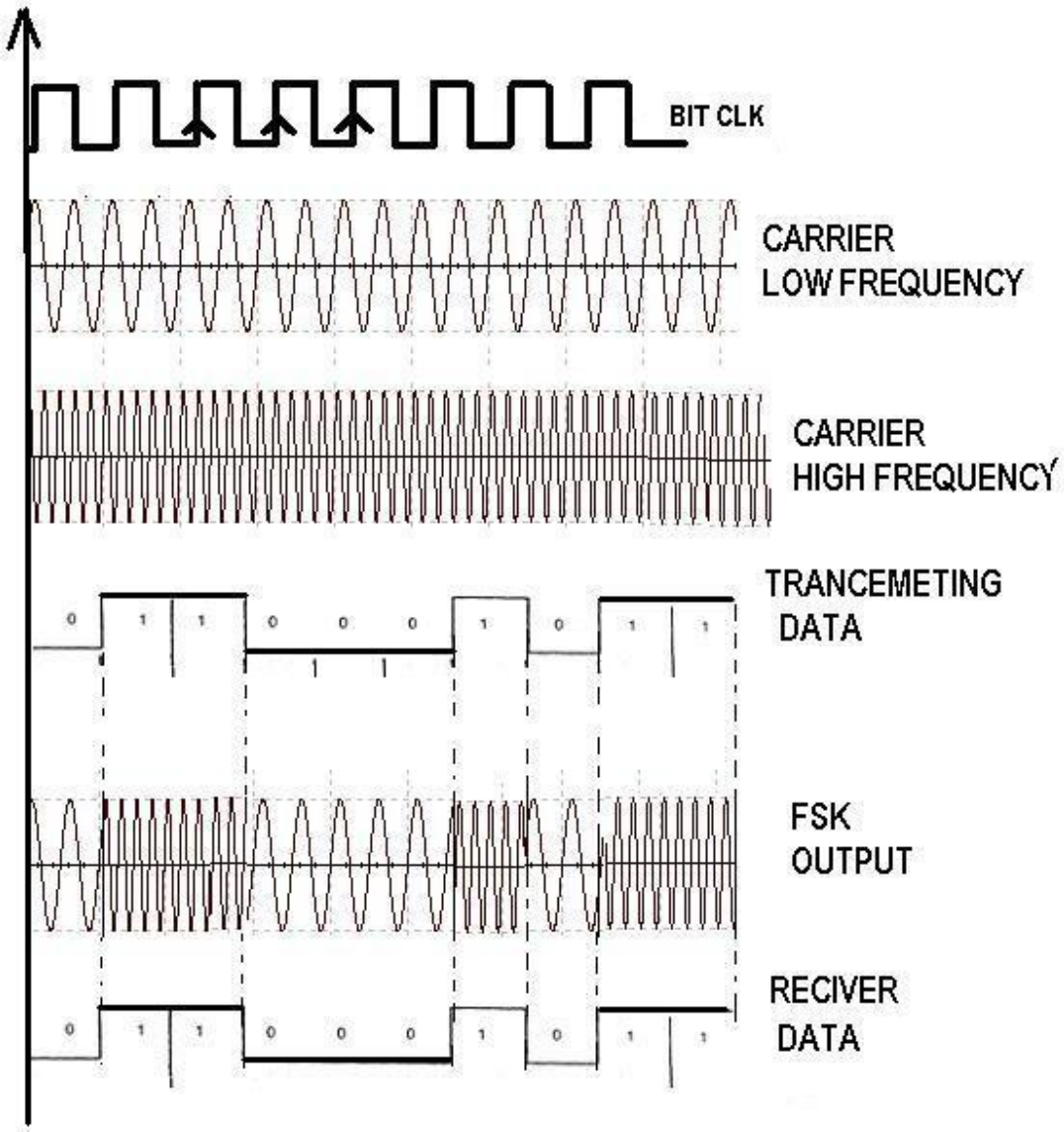


Figure 5.2 Output waveform of Frequency shift Keying

RESULT:

Applications

1. FM radio.
2. point-point military communications. 3.Telephone modem.

Viva Voce questions:

1. Define Binary FSK signal?
2. What is meant by carrier swing?
3. Define Frequency deviation of FSK signal?
4. What are the advantages of this FSK signal?
5. Give the differences between FSK & FM?

Sample questions

1. Explain how FSK works with the help of neat diagrams.
2. What is the bandwidth requirement of BPSK?
3. What is the expression for error probability of BPSK reception using coherent matched filter detection?
4. What are the draw backs of BPSK?
5. Draw the Power spectral density of BPSK

EXPERIMENT:12

BINARY PHASE SHIFT KEYING: GENERATION AND DETECTION

AIM: To study Binary Phase Shift Keying

Equipment Required

S. No	Name of Equipment	Model	Quantity
1	PSK trainer	AET-71	1
2	CRO	Analog	1
3	Multimeter	Digital	1
4	Connecting wires	BNC	2

CIRCUIT DIAGRAM

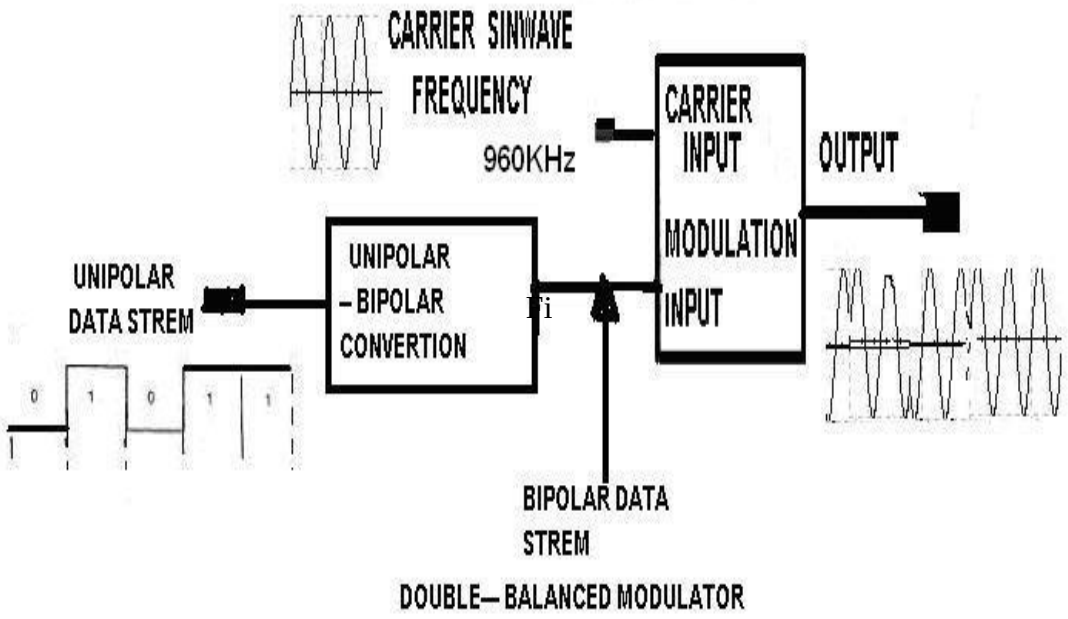


FIgure : Circuit Diagram of Phase Shift Keying

PROCEDURE:

x1Channel-0 i/p is connected to chennal-1 i/p

1. Mode switch is kept in fast mode.
2. Synch button is kept in on position.
3. Switched faults should be in OFF position.
4. Error check OFF (00).
5. Adjust the DC1 until the 7bit code displayed on A/D converter.

x

OUTPUT WAVEFORMS:

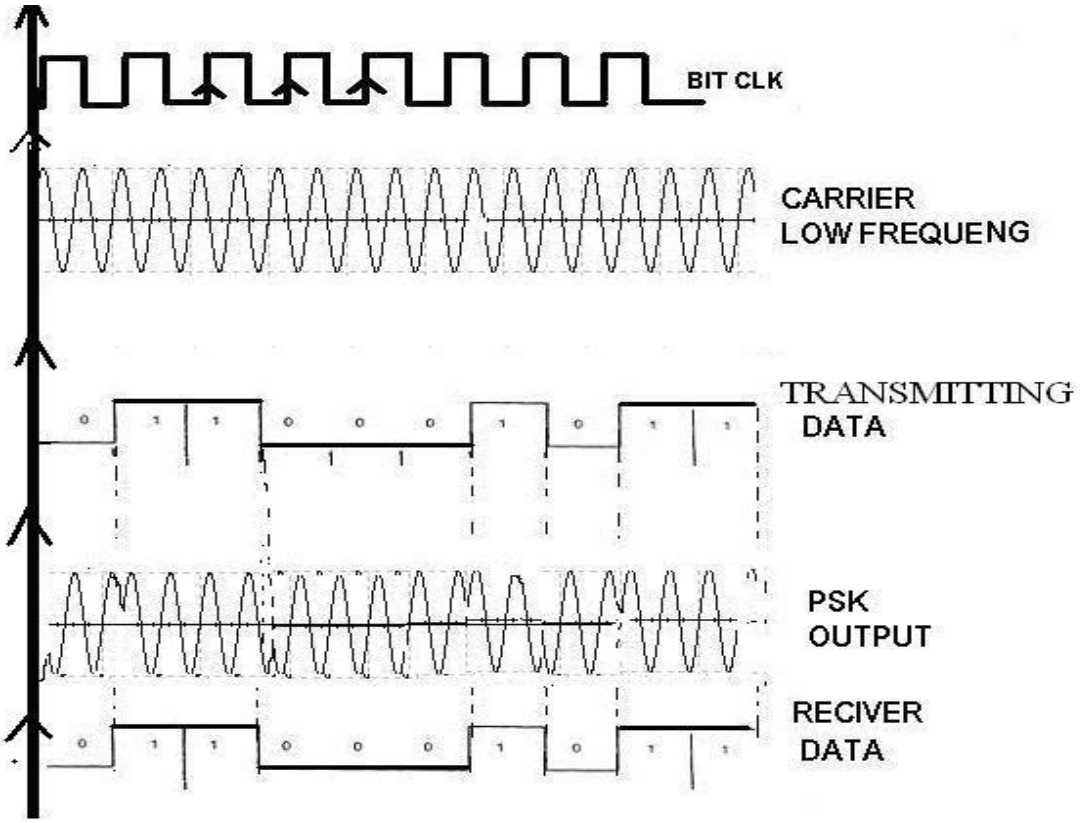


Figure 6.2 Output waveform of Phase Shift Keying

RESULT:

Applications

1. It is used in digital communications to modulate signals.

Viva Voce questions

1. What is the bandwidth requirement of BPSK?
2. What is the expression for error probability of BPSK reception using coherent matched filter detection?
3. What are the draw backs of BPSK?
4. Draw the Power spectral density of BPSK?
5. What are the major differences between DPSK&BPSK?

Sample questions:

a. Explain the operation of Phase Shift Keying (PSK) with the help of neat diagrams.
b. How PSK is different from FSK in principle.
c. What are major applications of PSK?
d. What are the major advantages of PSK over other shift keying techniques? What are the limitations of PSK?

EXPERIMENT:13

Generation and Detection (i) DPSK (ii) QPSK

i) **AIM:** To study the operation of Differential Phase Shift Keying

Equipment Required

S. No	Name of Equipment	Model	Quantity
1	DPSK trainer	AET-71	1
2	CRO	Analog	1
3	Multimeter	Digital	1
4	Connecting wires	BNC	2

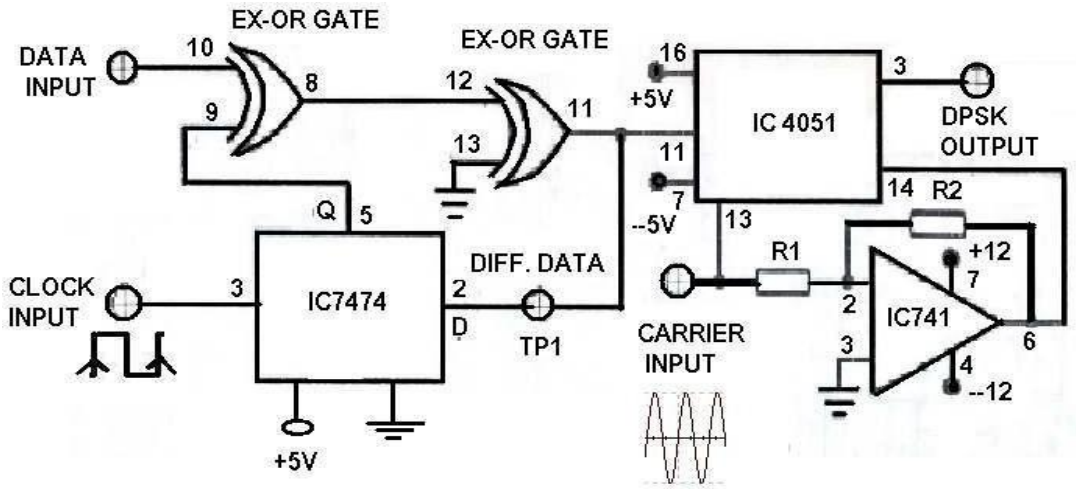
PREAMBLE:

We may view DPSK as the non-coherent vision of PSK. It eliminates the need for adjustment coherent reference signal at the receiver by connecting two basic operations at the transmitter.

1. Differential encoding at the transmitter.
2. Phase shift keying

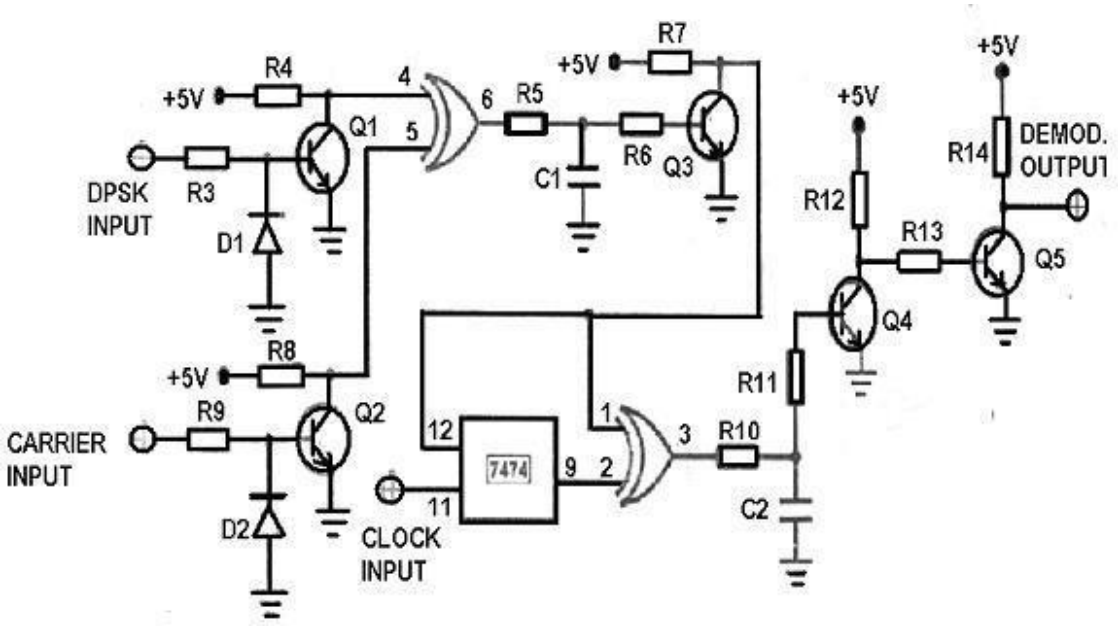
Hence differential encoding means the given input data will be done EX-OR operation with the previous encoded bit. Now the process of Phase shift keying will be done for both differentially encoded data and the carrier signal.

BLOCK DIAGRAM:



DPSK MODULATOR

Figure 8.1 Block Diagram of Differential Phase shift keying



DPSK DEMODULATOR

Figure 9.20.2 Block diagram of DPSK Demodulator

PROCEDURE:

(MODULATOR)

1. In this DPSK trainer kit there three signal generators one is for carrier signal and the second is for clock signal and another is for electrical representation of data bits, so give the carrier signal to CARRIER IN terminal OF MODULATOR.
2. Give the clock signal to CLOCK IN terminal and there are four different data bit combinations are available in the form of (D1, D2, D3 and D4) so connect one of this input data signal to DATA IN terminal of the modulator.
3. Take the differential data output across the DIFF.OUT terminal of the modulator.

4. And then observe the differentially phase shifted carrier signal across the output of the modulator i.e. DPSK output.

(DEMODULATOR)

5. Connect DPSK output to DPSK input terminal of the demodulator block.
6. Give the clock signal to CLOCK IN terminal and also connect the carrier signal to CARRIER IN terminal.
7. Ground both the modulator and demodulator circuits.
8. Observe the DPSK demodulated output across the DEMOD.OUT terminal of the demodulator circuit.

OUTPUT WAVE FORMS:

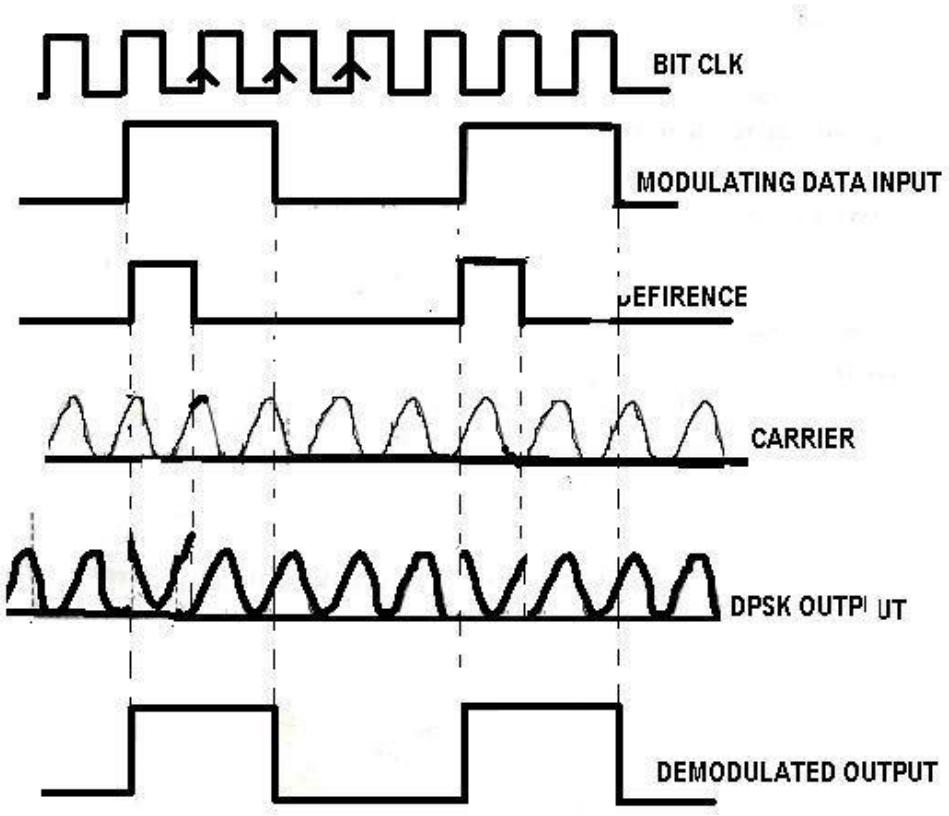


Figure 8.3 Output waveform of Differential Phase shift Keying

Result:

Applications

1. in radio communications.

Viva Voce questions:

1. Explain differences between DPSK and PSK systems
2. Explain DPSK system with its transmitter receiver and signal space representation
3. Explain the mechanism of DPSK
4. Explain the band width requirements of DPSK
5. What are the advantages of DPSK

Sample questions:

1. Explain differences between DPSK and PSK systems
2. Explain DPSK system with its transmitter receiver and signal space representation
3. Explain the block diagram of DPSK modulator and demodulator
4. Explain the band width requirements of DPSK. What are the applications of DPSK.What are the advantage of DPSK

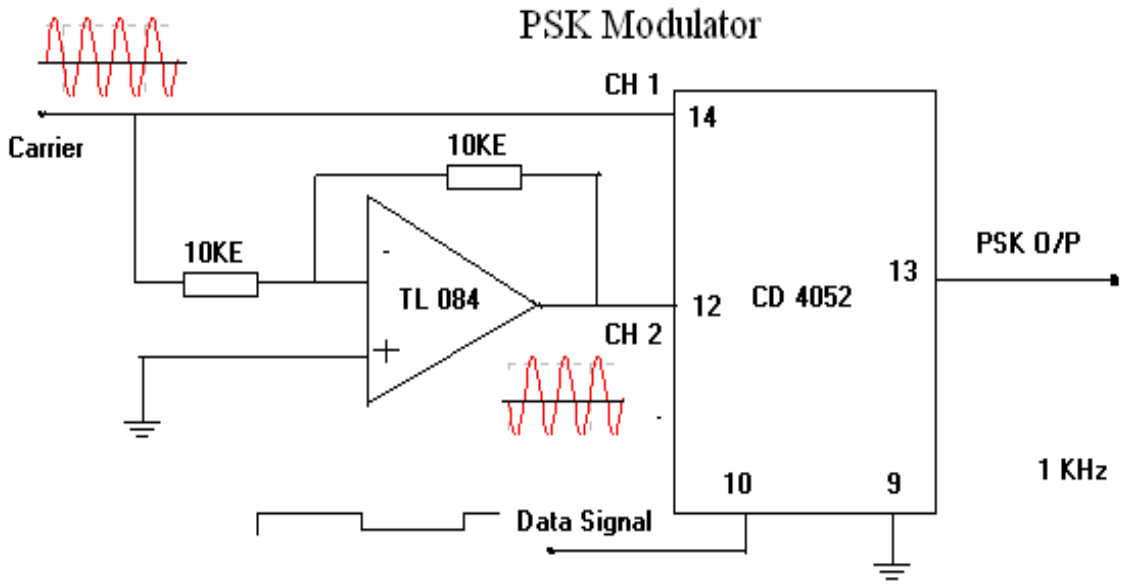
ii) **AIM:** Study the operation of QPSK (Binary) Modulation & Demodulation and to plot the QPSK wave forms for Binary data at different frequencies.

APPARATUS:

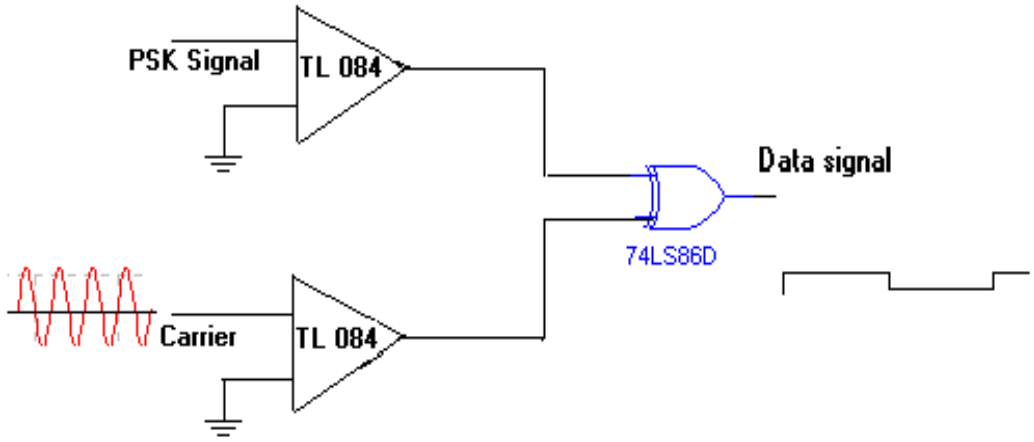
1. Quadrature Phase Shift keying trainer
2. Dual trace Oscilloscope
3. Digital multimeter
4. Patch chords

THEORY: Phase Shifting Keying (PSK) is a modulating / Data transmitting technique in which phase of the carrier signal is shifted between two distinct levels. In a simple PSK (i.e. Binary PSK) unshifted carrier Vcos $W_o t$ is transmitted to indicate a 1 condition, and the carrier shifted by 180 ^{o} i.e. -V cos $W_o t$ is transmitted to indicate a 0 condition. Wave forms are shown in Figure PSK Modulating & Demodulating circuitry can be developed in number of ways; one of the simple circuits is used in this trainer.

BLOCK DIAGRAM:



PSK Demodulator



PROCEDURE:

1. Study the theory of operation.
2. Connect the trainer to mains and switch on the power supply.
3. Measure the output of the regulated power supply i.e +5V and -5V with the help of digital multimeter.
4. Observe the output of the carrier generator using CRO, it should be an 8 KHz Sine with 5 Vpp amplitude.
5. Observe the various data signals (1 KHz, 2 KHz and 4 KHz) using CRO.

Modulation

6. Connect carrier signal to carrier input of the QPSK Modulator.
7. Connect data signal say 4 KHz from data source to data input of the modulator.
8. Keep CRO in dual mode.
9. Connect CH1 input of the CRO to data signal and CH2 to the output of the QPSK Modulator
10. Observe the QPSK o/p Signal with respect to data signal and plot the wave forms Compare the plotted waveforms with given wave forms.

Demodulation:

11. Connect the QPSK output to the QPSK input of the demodulator.
12. Connect carrier to the carrier input of the QPSK demodulator
    Note: In actual communication system reference carrier is generated at receiver.
13. Keep CRO in dual mode.

14. Connect CH1 to the data signal (at Modulator) and CH2 to the output of the demodulator.
15. Compare the demodulated signal with original data signal, By this we can notice that there is no loss in modulation and demodulation process.
16. Repeat the steps 7 to 15 with different data signals i.e 2 KHz and 1 KHz.

EXPECTED WAVEFORMS:

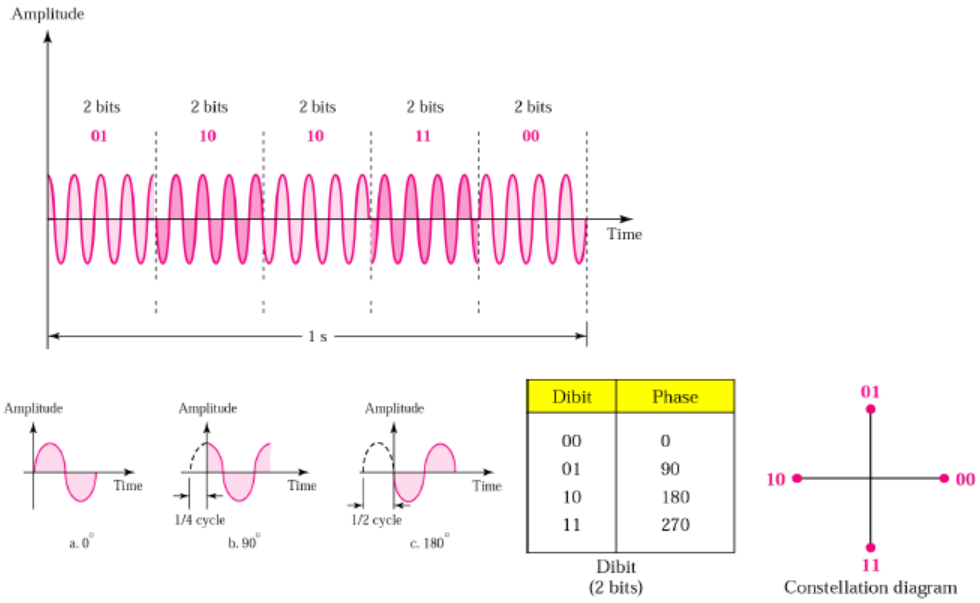


Fig4.3: QPSK output signal with constellation diagram

RESULT: The operation of QPSK (Binary) Modulation & Demodulation is verified and the QPSK wave forms for Binary data at different frequencies are plotted

VIVA QUESTIONS:

1. Explain the difference between PSK, DPSK and QPSK
2. Explain the difference between DPSK and QPSK
3. Define M-array signaling
4. Explain coherent method of PSK
5. Explain non-coherent method of PSK
6. Find the probability of error QPSK
7. What are the errors in QPSK

EXPERIMENT NO-1

AMPLITUDE MODULATION AND DEMODULATION (II) SPECTRUM ANALYSIS OF AM

AIM: To simulate amplitude modulation and demodulation using MATLAB/OCTAVE

APPARATUS:

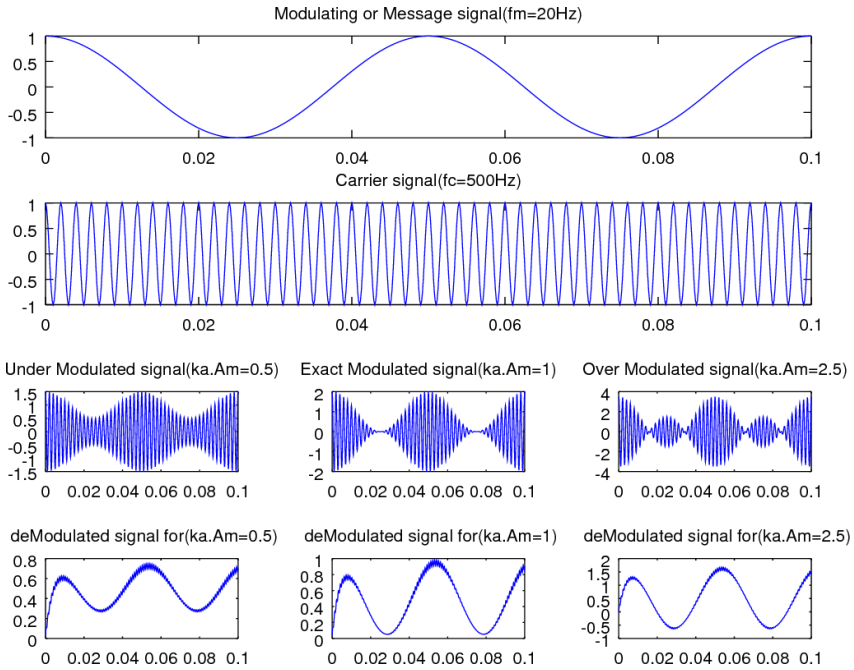
1. PC with windows (95/98/XP/NT/2000)
2. MATLAB/OCTAVE Software with communication toolbox

PROGRAM:

```
% program for AM modulation and demodulation close all
clear all clc fs=8000;
fm=20;
fc=500; Am=1; Ac=1;
t=[0:0.1*fs]/fs; m=Am*cos(2*pi*fm*t); c=Ac*cos(2*pi*fc*t); ka=0.5;
u=ka*Am; s1=Ac*(1+u*cos(2*pi*fm*t)).*cos(2*pi*fc*t); subplot(4,3,1:3);
plot(t,m);
title('Modulating or Message signal(fm=20Hz)'); subplot(4,3,4:6);
plot(t,c);
title('Carrier signal(fc=500Hz)'); subplot(4,3,7);
plot(t,s1);
title('Under Modulated signal(ka.Am=0.5)'); Am=2;
ka=0.5;
u=ka*Am; s2=Ac*(1+u*cos(2*pi*fm*t)).*cos(2*pi*fc*t); subplot(4,3,8);
plot(t,s2);
title('Exact Modulated signal(ka.Am=1)'); Am=5;
ka=0.5;

u=ka*Am;

s3=Ac*(1+u*cos(2*pi*fm*t)).*cos(2*pi*fc*t); subplot(4,3,9);
plot(t,s3);
title('Over Modulated signal(ka.Am=2.5)'); r1= s1.*c;
[b a] = butter(1,0.01); mr1= filter(b,a,r1); subplot(4,3,10);
plot(t,mr1);
title(' demodulated signal for(ka.Am=0.5)'); r2= s2.*c;
[b a] = butter(1,0.01); mr2= filter(b,a,r2); subplot(4,3,11);
plot(t,mr2);
```

```
title(' demodulated signal for(ka.Am=1)'); r3= s3.*c;
[b a] = butter(1,0.01); mr3= filter(b,a,r3); subplot(4,3,12);
plot(t,mr3);
title(' demodulated signal for(ka.Am=2.5)');
```

EXPECTED WAVES:



RESULT

EXPERMENT NO-2

FREQUENCY MODULATION AND DEMODULATION (II) SPECTRUM ANALYSIS OF FM

AIM: To simulate Frequency modulation and demodulation using MATLAB/OCTAVE

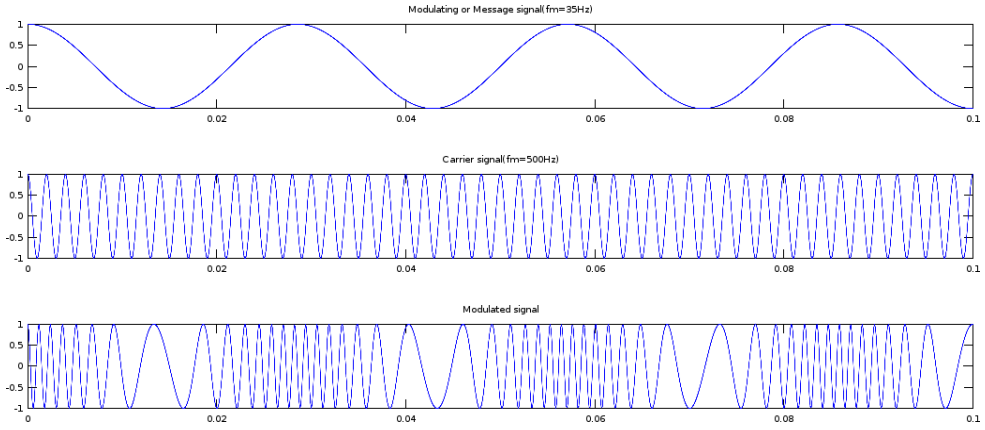
APPARATUS:

1. PC with windows (95/98/XP/NT/2000)
2. MATLAB/OCTAVE Software with communication toolbox

PROGRAM: -

```
% program for fm modulation and demodulation close all
clear all clc
%fm=35HZ,fc=500HZ,Am=1V,Ac=1V,B=10 fs=10000;
Ac=1; Am=1;
fm=35; fc=500; B=10;
t=(0:.1*fs)/fs; wc=2*pi*fc; wm=2*pi*fm; m_t=Am*cos(wm*t); subplot(4,1,1);
plot(t,m_t);
title('Modulating or Message signal(fm=35Hz)'); c_t=Ac*cos(wc*t);
subplot(4,1,2);
plot(t,c_t);
title('Carrier signal(fm=500Hz)'); s_t=Ac*cos((wc*t)+B*sin(wm*t)); subplot(4,1,3);
plot(t,s_t); title('Modulated signal'); d=demod(s_t,fc,fs,'fm'); subplot(4,1,4);
plot(t,d); title('demodulated signal');
```

EXPECTED WAVEFORMS



RESULT

EXPERIMENT NO-3

DSB-SC MODULATOR & DETECTOR

AIM: To simulate DSB-SC modulation and demodulation using MATLAB/OCTAVE

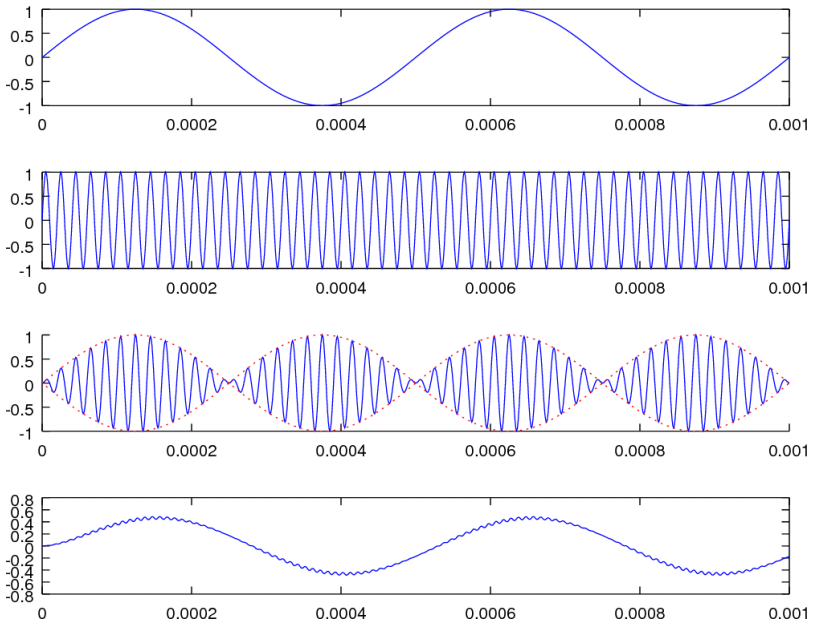
APPARATUS:

1. PC with windows (95/98/XP/NT/2000)
2. MATLAB/OCTAVE Software with communication toolbox

PROGRAM:

```
% program for dsbsc modulation and demodulation close all
clear all clc
t =0:0.000001:.001;
Vm= 1;
Vc= 1;
fm = 2000;
fc= 50000;
m_t = Vm*sin(2*pi*fm*t); subplot(4,1,1);
plot(t,m_t);
c_t = Vc*sin(2*pi*fc*t); subplot(4,1,2);
plot(t,c_t);
subplot(4,1,3); s_t = m_t.*c_t; hold on; plot(t,s_t); plot(t,m_t,'r:');
plot(t,-m_t,'r:'); hold off;
r = s_t.*c_t;
[b a] = butter(1,0.01); mr= filter(b,a,r); subplot(4,1,4);
plot(t,mr);
```

EXPECTED WAVEFORMS



RESULT

EXPERIMENT.NO-4

SSB-SC MODULATOR & DETECTOR (PHASE SHIFT METHOD)

AIM: To simulate SSB-SC modulation and demodulation using MATLAB/OCTAVE

APPARATUS:

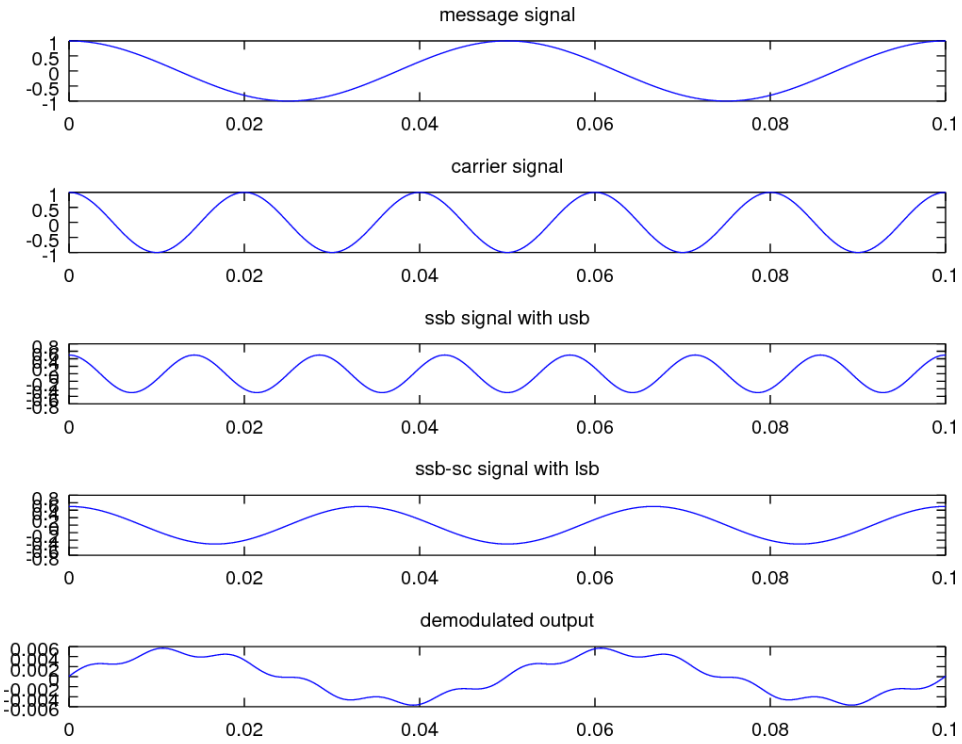
1. PC with windows (95/98/XP/NT/2000)
2. MATLAB/OCTAVE Software with communication toolbox

PROGRAM:-

```
% program for ssb modulation and demodulation close all
clear all clc fs=8000;
fm=20; fc=50; Am=1; Ac=1;
t=[0:0.1*fs]/fs;
subplot(5,1,1); m1=Am*cos(2*pi*fm*t); plot(t,m1);
title('Message Signal'); m2=Am*sin(2*pi*fm*t); subplot(5,1,2)
c1=Ac*cos(2*pi*fc*t);
plot(t,c1) title('Carrier Signal');
c2=Ac*sin(2*pi*fc*t); subplot(5,1,3)
% Susb=0.5* Am*cos(2*pi*fm*t).* Ac*cos(2*pi*fc*t) -- 0.5* Am*sin(2*pi*fm*t).* Ac*sin(2*pi*fc*t);
Susb=0.5*m1.*c1-0.5*m2.*c2; plot(t,Susb);
title('SSB-SC Signal with USB'); subplot(5,1,4); Slsb=0.5*m1.*c1+0.5*m2.*c2; plot(t,Slsb);
title('SSB-SC Signal with LSB'); r = Susb.*c1;
```

```
subplot(5,1,5);
[b a] = butter(1,0.0001); mr= filter(b,a,r); plot(t,mr); title('demodulated output');
```

EXPECTED WAVEFORMS



RESULT

EXPERIMENT NO-5

FREQUENCY DIVISION MULTIPLEXING & DEMULTIPLEXING

AIM: To simulate Frequency division multiplexing and de multiplexing using MATLAB/OCTAVE

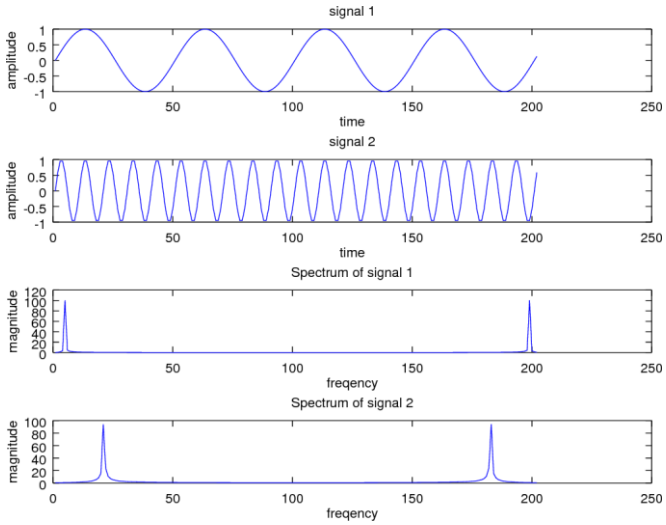
APPARATUS:

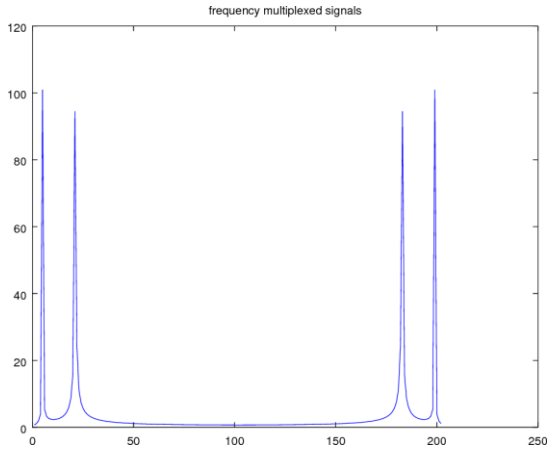
1. PC with windows (95/98/XP/NT/2000)
2. MATLAB/OCTAVE Software with communication toolbox

PROGRAM:

```
%program for frequency division multiplexing and demultiplexing close all
clear all clc
Fs = 100; % sampling freq t = [0:2*Fs+1]'/Fs;
x1 = sin(2*pi*2*t); % signal 1 signal z1 = fft(x1);
z1=abs(z1);
x2 = sin(2*pi*10*t); % signal 2 signal z2 = fft(x2);
z2=abs(z2); figure;
subplot(4,1,1); plot(x1);
title('signal 1');xlabel('time');ylabel('amplitude'); subplot(4,1,2); plot(x2);
title('signal 2');xlabel('time');ylabel('amplitude'); subplot(4,1,3); plot(z1);
title('Spectrum of signal 1');xlabel('freqency');ylabel('magnitude'); subplot(4,1,4); plot(z2);
title('Spectrum of signal 2');xlabel('freqency');ylabel('magnitude');
% freqency multiplexing z=z1+z2;
figure; plot(z);
title('frequency multiplexed signals');
figure;
% freqency demultiplexing
f1=[ones(10,1); zeros(182,1);ones(10,1)];%applying filter for signal 1 dz1=z.*f1;
d1 = ifft(dz1); subplot(2,1,1) plot(t*100,d1);
f2=[zeros(10,1); ones(182,1);zeros(10,1)];% applying filter for signal 2 dz2=z.*f2;
d2 = ifft(dz2);
title('recovered signal 1');xlabel('time');ylabel('amplitude'); subplot(2,1,2)
plot(t*100,d2);
title('recovered signal 2');xlabel('time');ylabel('amplitude');
```

EXPECTED WAVEFORMS:





RESULT

EXPERIMENT NO-6

PULSE AMPLITUDE MODULATION & DEMODULATION

AIM: To simulate pulse amplitude modulation using MATLAB/OCTAVE

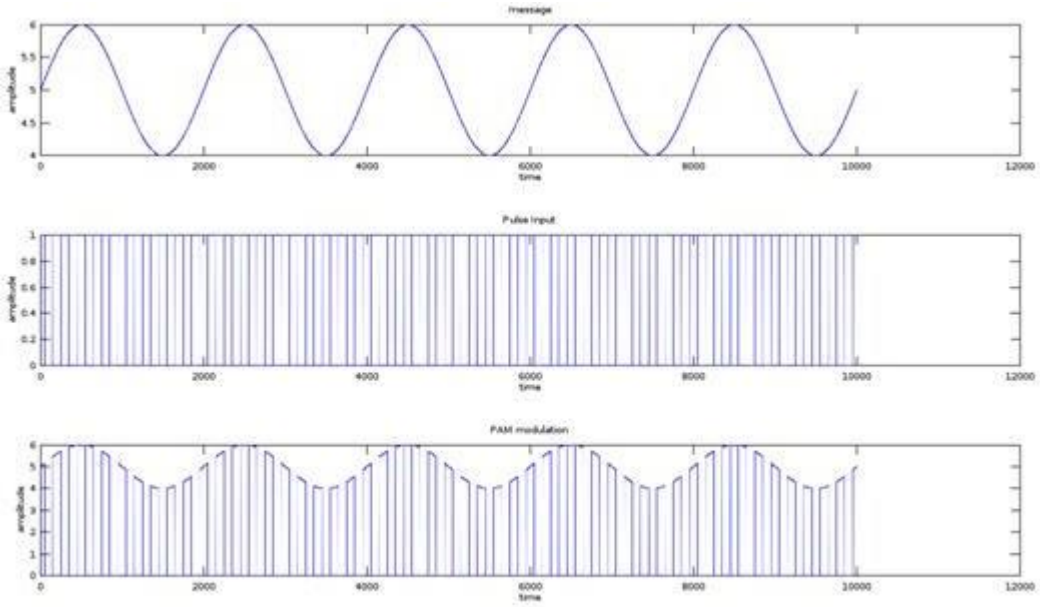
APPARATUS:

1. PC with windows (95/98/XP/NT/2000)
2. MATLAB/OCTAVE Software with communication toolbox

PROGRAM:-

```
% pulse amplitude modulation close all

clear all clc

t = 0 : 1/1e3 : 10; % 1 kHz sample freq for 1 sec d = 0 : 1/5 : 10;

x = 5+sin(2*pi/4*2*t); %message signal figure;

subplot(3,1,1) plot(x); title('message');

xlabel('time');ylabel('amplitude');

y = pulstran(t,d,'rectpuls',0.1); %generation of pulse input subplot(3,1,2)

plot(y);

title('Pulse Input '); xlabel('time');ylabel('amplitude');

z=x.*y; % PAM output subplot(3,1,3)

plot(z);

title('PAM modulation '); xlabel('time');ylabel('amplitude');
```

EXPECTED WAVEFORMS



RESULT

EXPERIMENT NO-7
PULSE WIDTH MODULATION & DEMODULATION

AIM: To simulate pulse width modulation using MATLAB/OCTAVE

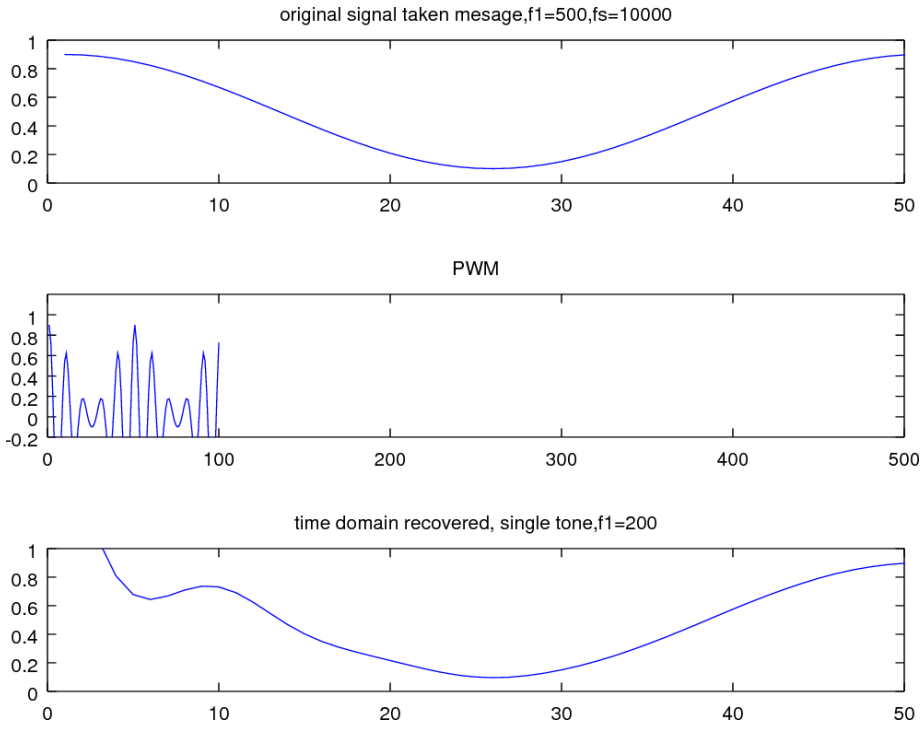
APPARATUS:

1. PC with windows (95/98/XP/NT/2000)
2. MATLAB/OCTAVE Software with communication toolbox

PROGRAM:-

```
% pulse width modulation & demodulation close all
clear all clc fc=1000; fs=10000; f1=200;
t=0:1/fs:((2/f1)-(1/fs)); x1=0.4*cos(2*pi*f1*t)+0.5;
%modulation y1=modulate(x1,fc,fs,'pwm'); subplot(311);
plot(x1); axis([0 50 0 1]);
title('original signal taken mesage,f1=500,fs=10000') subplot(312);
plot(y1);
axis([0 500 -0.2 1.2]);
title('PWM')
%demodulation x1_recov=demod(y1,fc,fs,'pwm'); subplot(313);
plot(x1_recov);
title('time domain recovered, single tone,f1=200') axis([0 50 0 1]);
```

EXPECTED WAVEFORMS:



RESULT

EXPERIMENT NO-8
PULSE POSITION MODULATION AND DEMODULATION

AIM: To simulate pulse position modulation using MATLAB/OCTAVE

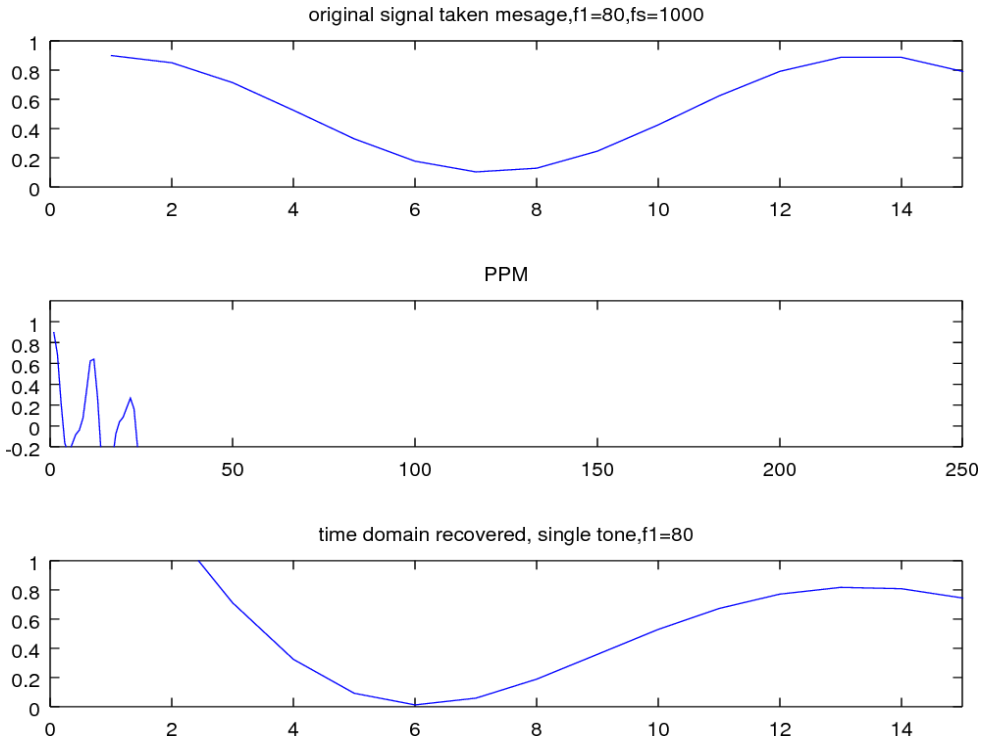
APPARATUS:

1. PC with windows (95/98/XP/NT/2000)
2. MATLAB/OCTAVE Software with communication toolbox

PROGRAM:-

```
% pulse position modulation close all

clear all clc fc=100; fs=1000; f1=80;

t=0:1/fs:((2/f1)-(1/fs)); x1=0.4*cos(2*pi*f1*t)+0.5;

%modulation y1=modulate(x1,fc,fs,'ppm'); subplot(311);

plot(x1); axis([0 15 0 1]);

title('original signal taken mesage,f1=80,fs=1000') subplot(312);

plot(y1);

axis([0 250 -0.2 1.2]);

title('PPM')

%demodulation x1_recov=demod(y1,fc,fs,'ppm'); subplot(313);

plot(x1_recov);

title('time domain recovered, single tone,f1=80') axis([0 15 0 1]);
```

EXPECTED WAVEFORMS:



RESULT

EXPERIMENT NO-9

PCM GENERATION AND DETECTION

AIM: To simulate Pulse Code modulation using MATLAB/OCTAVE

APPARATUS:

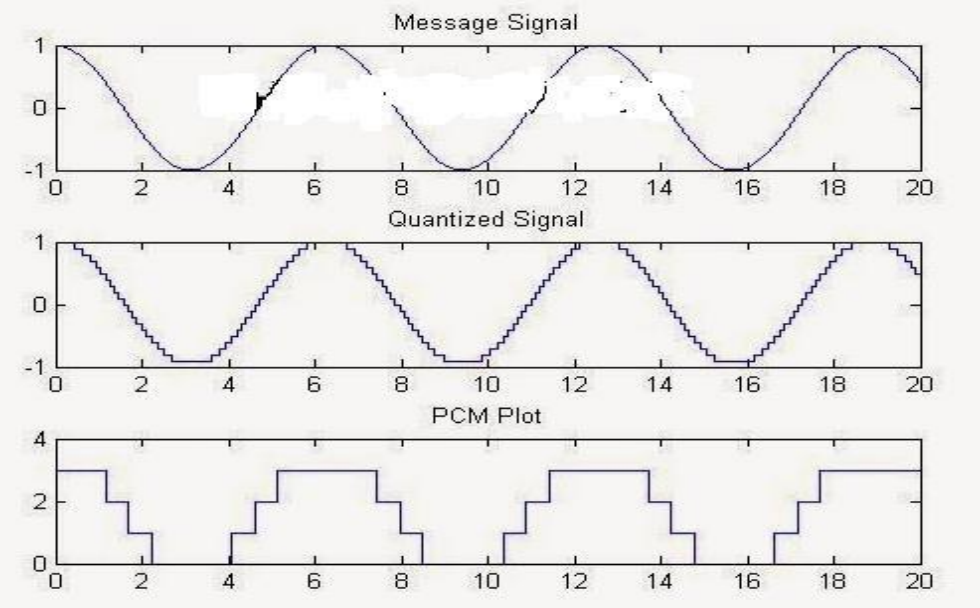
1. PC with windows (95/98/XP/NT/2000)
2. MATLAB/OCTAVE Software with communication toolbox

PROGRAM:-

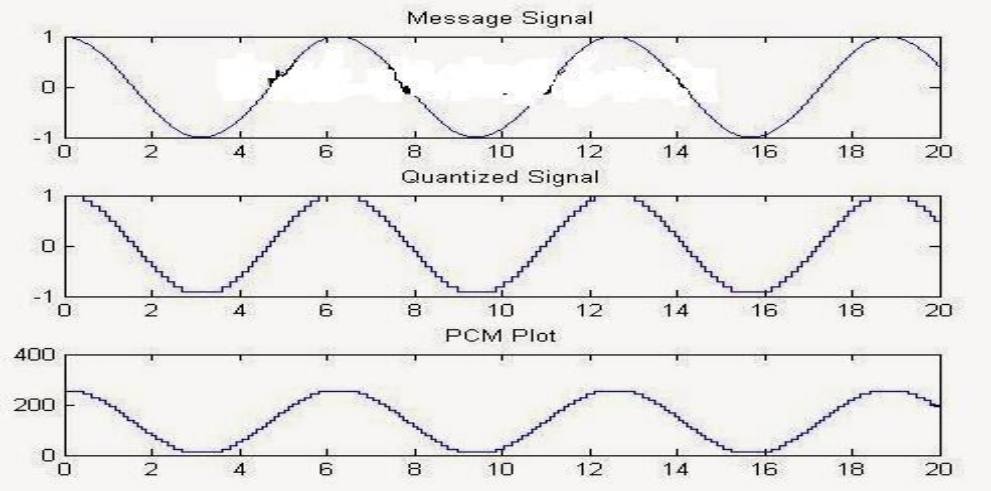
```
clc close all clear all
t = 0:0.0001:20; %sampling at niquist rate c=input('Enter Bit Depth Of PCM Coding:');
part = -1:0.1:1;%A quantization partition defines several contiguous, nonoverlapping ranges
%of values within the set of real numbers.
codebook = -1:0.1:1.1;%A codebook tells the quantizer which common value to assign to inputs that
%fall into each range of the partition. msg = cos(t);
[~,quants] = quantiz(msg,part,codebook);%returns a vector that tells which interval each input is in
subplot(3,1,1);
plot(t,msg); title('Message Signal'); subplot(3,1,2); plot(t,quants); title('Quantized Signal'); y =
uencode(quants,c);
ybin=dec2bin(y,c); %converting it to final binary form to make it transmit ready subplot(3,1,3);
plot(t,y); title('PCM PLOT');
```

EXPECTED WAVEFORMS:

Enter Bit Depth Of PCM Coding:2



Enter Bit Depth Of PCM Coding:8



RESULT:

EXPERIMENT NO-10

DELTA MODULATION

AIM: To simulate Delta Modulation using MATLAB/OCTAVE

APPARATUS:

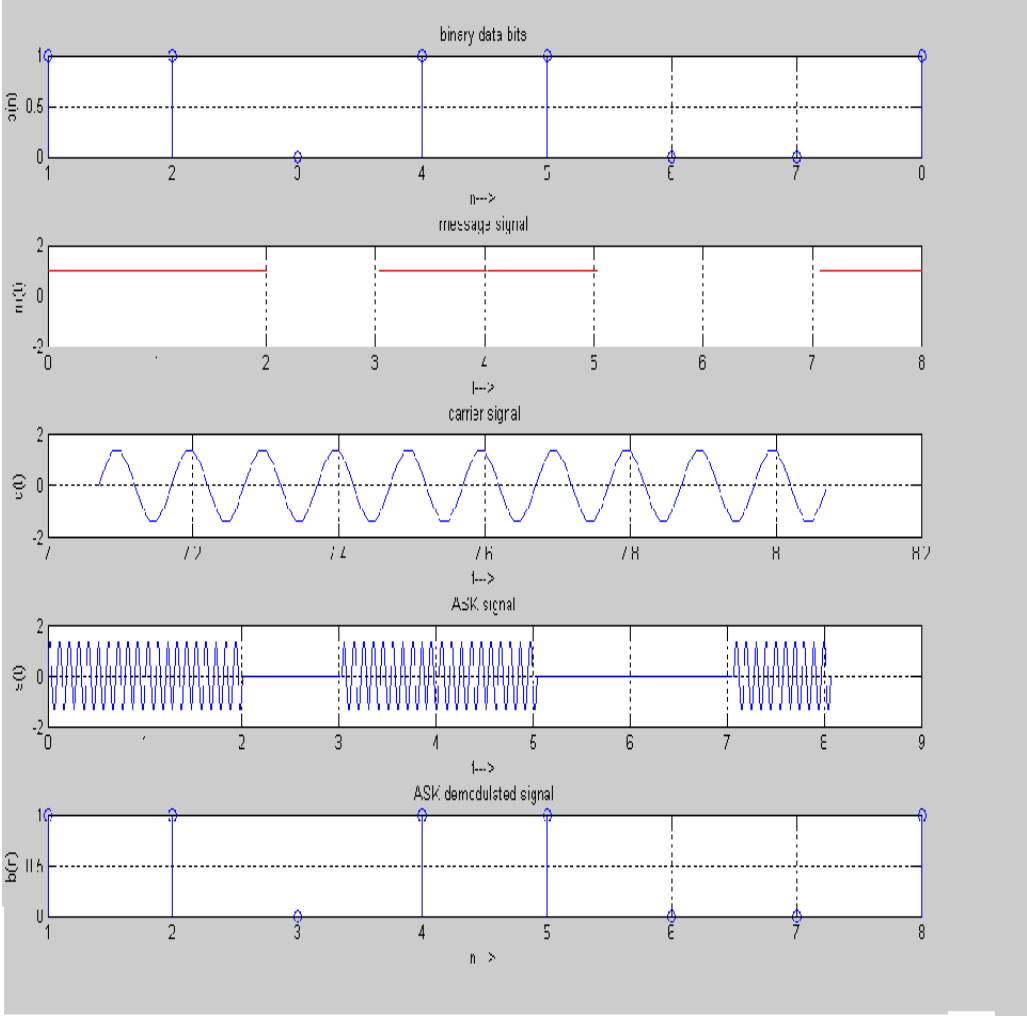
1. PC with windows (95/98/XP/NT/2000)
2. MATLAB/OCTAVE Software with communication toolbox

PROGRAM:-

```
%ASK Modulation

clc; clear all; close all;
%GENERATE CARRIER SIGNAL Tb=1; fc=10;
t=0:Tb/100:1;
c=sqrt(2/Tb)*sin(2*pi*fc*t);
%generate message signal N=8;
m=rand(1,N); t1=0;t2=Tb for i=1:N t=[t1:.01:t2]
if m(i)>0.5 m(i)=1;
m_s=ones(1,length(t)); else
m(i)=0;
m_s=zeros(1,length(t)); end
message(i,:)=m_s;
%product of carrier and message ask_sig(i,:)=c.*m_s; t1=t1+(Tb+.01); t2=t2+(Tb+.01);
%plot the message and ASK signal subplot(5,1,2);axis([0 N -2 2]);plot(t,message(i,:),'r');
title('message signal');xlabel('t--->');ylabel('m(t)');grid on hold on
subplot(5,1,4);plot(t,ask_sig(i,:));

title('ASK signal');xlabel('t--->');ylabel('s(t)');grid on hold on
end hold off
%Plot the carrier signal and input binary data subplot(5,1,3);plot(t,c);
title('carrier signal');xlabel('t--->');ylabel('c(t)');grid on subplot(5,1,1);stem(m);
title('binary data bits');xlabel('n--->');ylabel('b(n)');grid on
%  Demodulation
t1=0;t2=Tb for i=1:N
t=[t1:Tb/100:t2]
%correlator x=sum(c.*ask_sig(i,:));
%decision device if x>0 demod(i)=1;

else demod(i)=0; end t1=t1+(Tb+.01); t2=t2+(Tb+.01);
end
%plot demodulated binary data bits subplot(5,1,5);stem(demod);
```

title('ASK demodulated signal'); xlabel('n--->');ylabel('b(n)');grid on

EXPECTED WAVEFORM



RESULT:

EXPERIMENT NO-11

FREQUENCY SHIFT KEYING: GENERATION AND DETECTION

AIM: To simulate FSK Modulation using MATLAB/OCTAVE

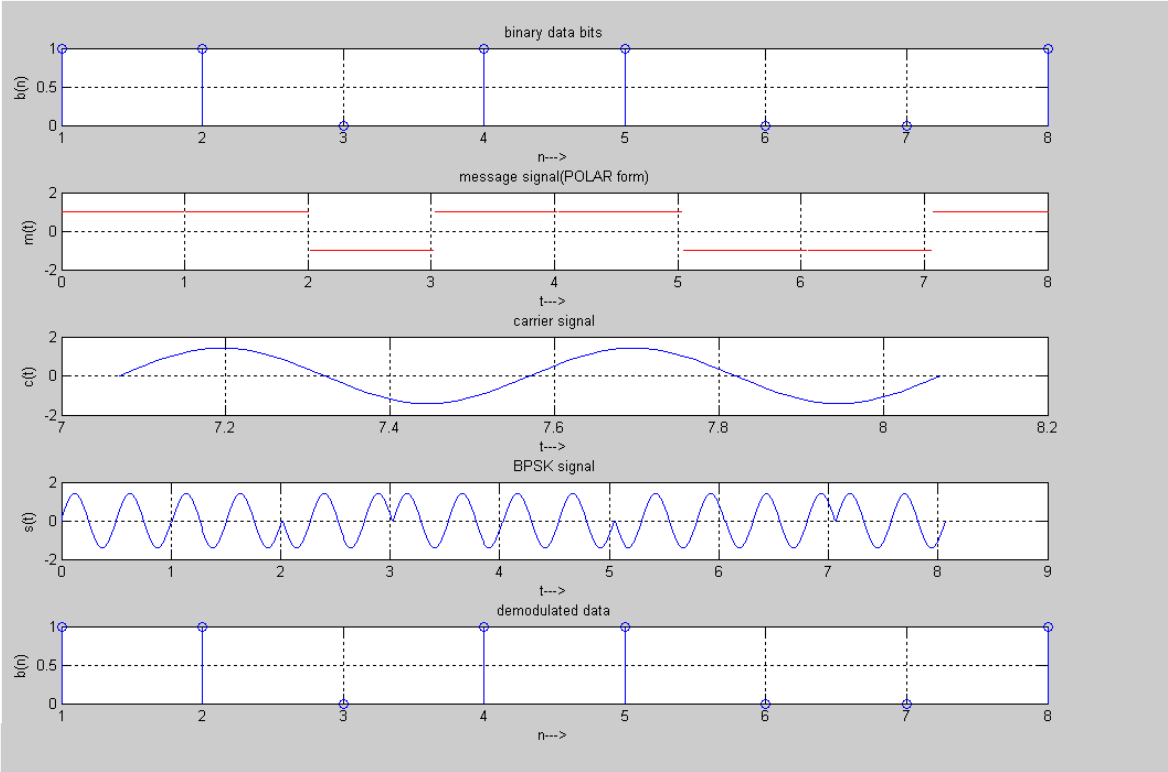
APPARATUS:

1. PC with windows (95/98/XP/NT/2000)
2. MATLAB/OCTAVE Software with communication toolbox

PROGRAM:-

```
% FSK modulation
clc; clear all; close all;
%GENERATE CARRIER SIGNAL Tb=1;
t=0:Tb/100:Tb;
fc=2; c=sqrt(2/Tb)*sin(2*pi*fc*t);
%generate message signal N=8;
m=rand(1,N); t1=0;t2=Tb for i=1:N t=[t1:.01:t2]
if m(i)>0.5 m(i)=1;
m_s=ones(1,length(t)); else
m(i)=0;
m_s=-1*ones(1,length(t)); end
message(i,:)=m_s;
%product of carrier and message signal bpsk_sig(i,:)=c.*m_s;
%Plot the message and BPSK modulated signal subplot(5,1,2);axis([0 N -2 2]);plot(t,message(i,:),'r');
title('message signal(POLAR form)');xlabel('t--->');ylabel('m(t)'); grid on; hold on;
subplot(5,1,4);plot(t,bpsk_sig(i,:)); title('BPSK signal');xlabel('t--->');ylabel('s(t)');

grid on; hold on;
```

EXPECTED WAVEFORM



RESULT

EXPERIMENT NO-12
BINARY PHASE SHIFT KEYING: GENERATION AND DETECTION

AIM: To simulate BPSK Modulation modulation using MATLAB/OCTAVE

APPARATUS:

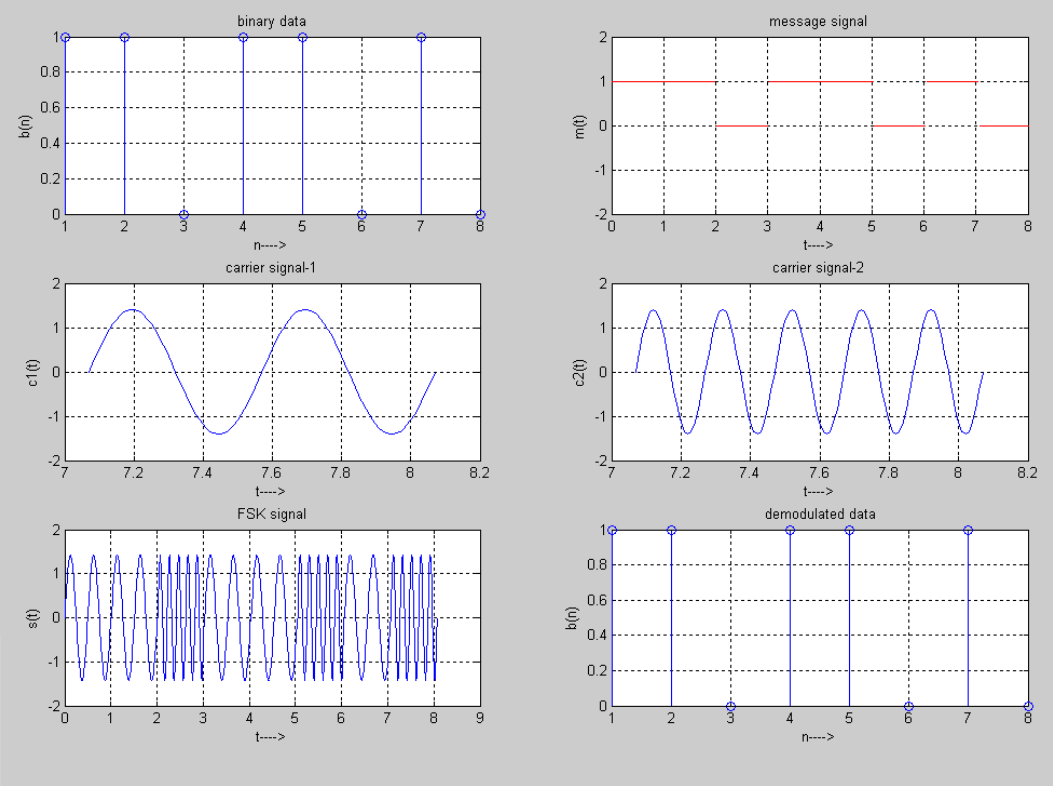
1. PC with windows (95/98/XP/NT/2000)
2. MATLAB/OCTAVE Software with communication toolbox

PROGRAM:-

```
clc; clear all; close all;
%GENERATE CARRIER SIGNAL Tb=1; fc1=2;fc2=5; t=0:(Tb/100):Tb;
c1=sqrt(2/Tb)*sin(2*pi*fc1*t); c2=sqrt(2/Tb)*sin(2*pi*fc2*t);
%generate message signal N=8;
m=rand(1,N); t1=0;t2=Tb for i=1:N
t=[t1:(Tb/100):t2]
if m(i)>0.5 m(i)=1;
m_s=ones(1,length(t)); invm_s=zeros(1,length(t)); else
m(i)=0;
m_s=zeros(1,length(t)); invm_s=ones(1,length(t)); end
message(i,:)=m_s;
%Multiplier fsk_sig1(i,:)=c1.*m_s; fsk_sig2(i,:)=c2.*invm_s; fsk=fsk_sig1+fsk_sig2;
%plotting the message signal and the modulated signal
```

```
subplot(3,2,2);axis([0 N -2 2]);plot(t,message(i,:),'r');
title('message signal');xlabel('t --->');ylabel('m(t)');grid on;hold on;
```

EXPECTED WAVEFORM:



RESULT:

EXPERIMENT NO-13

Generation and Detection (i) DPSK (ii) QPSK

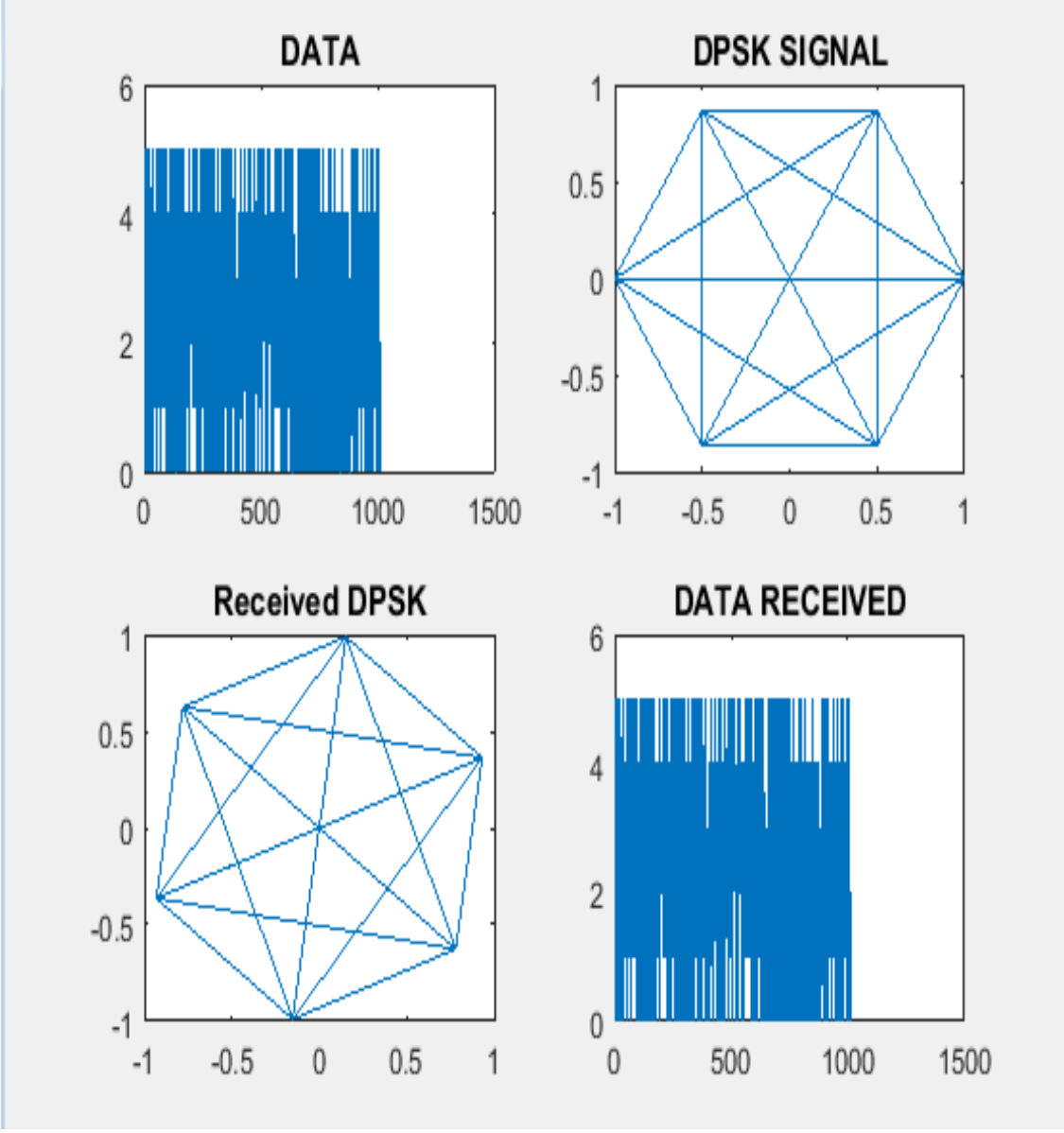
AIM: To simulate DPSK Modulation using MATLAB/OCTAVE

APPARATUS:

1. PC with windows (95/98/XP/NT/2000)
2. MATLAB/OCTAVE Software with communication toolbox

PROGRAM FOR DPSK GENERATION

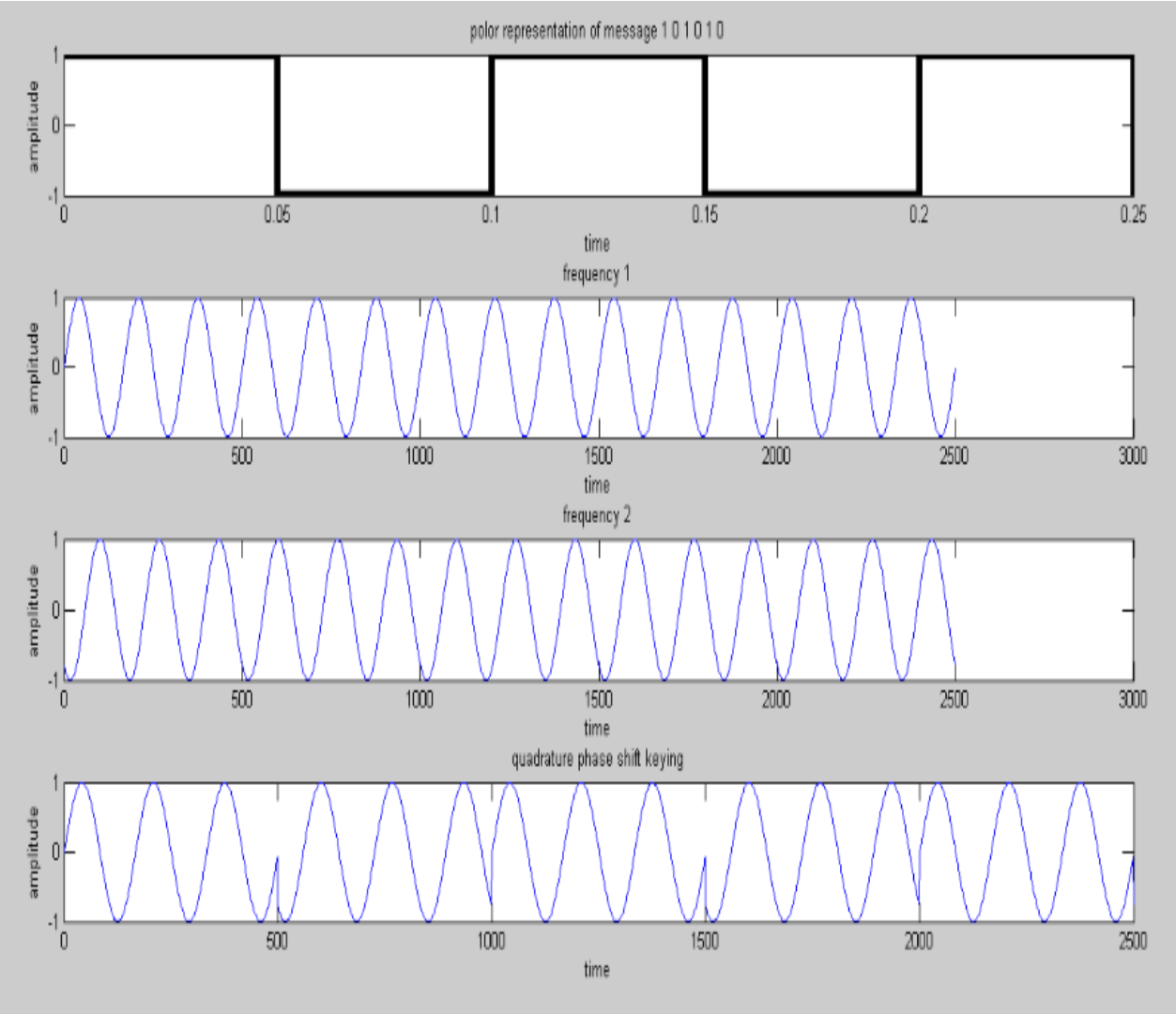
```
clear all; rng default
M = 6; % Alphabet size
dataIn = randi([0 M-1],1011,1); % Random message txSig = dpskmod(dataIn,M); % Modulate
rxSig = txSig*exp(2i*pi*rand()); dataOut = dpskdemod(rxSig,M); errs = symerr(dataIn,dataOut)
errs = symerr(dataIn(2:end),dataIn(2:end)) figure
subplot(2,2,1) plot(dataIn) title('DATA') subplot(2,2,2) plot(txSig) title('DPSK SIGNAL')
subplot(2,2,3) plot(rxSig) title('Received DPSK') subplot(2,2,4) plot(dataOut)
title('DATA RECEIVED')
```


DATA
DPSK SIGNAL
Received DPSK
DATA RECEIVED

PROGRAM FOR QPSK GENERATION

```
clc; clear all; t=0:0.0001:0.25;
m=square(2*pi*10*t); c1=sin(2*pi*60*t); c2=sin(2*pi*60*t+180); for i=1:2500 if(mod(i,1000))<500
s(i)=c1(i);
else
s(i)=-c2(i); end
end subplot(4,1,1);
plot(t,m,'k','linewidth',5);
title('polor representation of message 1 0 1 0 1 0'); xlabel('time'); ylabel('amplitude')
subplot(4,1,2); plot(c1); title('frequency 1');
xlabel('time'); ylabel('amplitude'); subplot(4,1,3); plot(c2); title('frequency 2');
xlabel('time'); ylabel('amplitude'); subplot(4,1,4); plot(s); title('quadrature phase shift keying');
xlabel('time');
ylabel('amplitude');
```

EXPECTED WAVEFORM:



RESULT:

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Department of Electronics and Communication Engineering

Academic Year: 2019-20 II B. Tech Semester: II Section-B

Day to Day lab evaluation **Name of the Lab:ADC LAB**

Roll No.: 18QM1AO462 Name of the Student:Mohammed AsnaKousar

S.No.	Name of the Experiment	Date of Experiment	Record of previous experiment (5 marks)	Execution of experiment (5 marks)	Viva-Voce (5 marks)	Total (15 marks)	Remarks by Faculty
1	(i) Amplitude modulation and demodulation (ii) Spectrum analysis of AM	31-12-2019	5	5	5	15	Excellent
2	(i) Frequency modulation and demodulation (ii) Spectrum analysis of FM	07-01-2020	5	5	5	15	Good
3	DSB-SC Modulator & Detector	31-12-2019	5	4	5	14	Good
4	SSB-SC Modulator & Detector (Phase Shift Method)	07-01-2020	5	5	5	15	Excellent
5	Frequency Division Multiplexing & De multiplexing	21-01-2020	5	5	5	15	Excellent
6	Pulse Amplitude Modulation & Demodulation	31-12-2019	5	4	5	14	Good
7	Pulse Width Modulation & Demodulation	21-01-2020	5	5	5	15	Excellent
8	Pulse Position Modulation & Demodulation	28-01-2020	5	5	5	15	Excellent
9	Delta Modulation	18-02-2020	5	5	5	15	Good
10	Frequency Shift Keying: Generation and Detection	25-02-2020	5	5	5	14	Good
11	Binary Phase Shift Keying: Generation and Detection	18-02-2020	5	5	5	15	Excellent
12	Generation and Detection (i) DPSK (ii) QPSK	25-02-2020	5	5	5	15	Excellent
	Average					15	Excellent

Faculty Member

HOD

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Academic Year: 2019-20

Department of Electronics and Communication Engineering

II B. Tech Semester: II

Section-B

Day to Day lab evaluation

Name of the Lab:ADC LAB

Roll No.: 18QM1AO465

Name of the Student: Morse Sathwika Reddy

S.No.	Name of the Experiment	Date of Experiment	Record of previous experiment (5 marks)	Execution of experiment (5 marks)	Viva-Voce (5 marks)	Total (15 marks)	Remarks by Faculty
1	(i) Amplitude modulation and demodulation (ii) Spectrum analysis of AM	31-12-2019	5	3	2	10	Improve on Viva and revise experiments
2	(i) Frequency modulation and demodulation (ii) Spectrum analysis of FM	07-01-2020	5	3	2	10	Improve on Viva and revise experiments
3	DSB-SC Modulator & Detector	31-12-2019	5	3	2	10	Improve on Viva and revise experiments
4	SSB-SC Modulator & Detector (Phase Shift Method)	07-01-2020	5	3	2	10	Improve on Viva and revise experiments
5	Frequency Division Multiplexing & De multiplexing	21-01-2020	4	3	2	9	Improve on Viva and revise experiments
6	Pulse Amplitude Modulation & Demodulation	28-01-2020	5	3	2	10	Improve on Viva and revise experiments
7	Pulse Width Modulation & Demodulation	28-01-2020	5	3	2	10	Improve on Viva and revise

							experiments
8	Pulse Position Modulation & Demodulation	31-12-2019	5	3	2	10	Improve on Viva and revise experiments
9	Delta Modulation	25-02-2020	4	3	2	9	Improve on Viva and revise experiments
10	Frequency Shift Keying: Generation and Detection	07-01-2020	5	3	2	10	Improve on Viva and revise experiments
11	Binary Phase Shift Keying: Generation and Detection	21-01-2020	5	3	2	10	Improve on Viva and revise experiments
12	Generation and Detection (i) DPSK (ii) QPSK	28-01-2020	5	3	2	10	Improve on Viva and revise experiments
	Average					10	Improve on Viva and revise experiments

Faculty Member

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Department of Electronics and Communication Engineering

Academic Year: 2019-20 II B. Tech Semester: II Section-B

Day to Day lab evaluation

Name of the Lab:ADC LAB

Roll No.: 18QM1AO466 **Name of the Student:MudhavathPavanNayak**

S.No.	Name of the Experiment	Date of Experiment	Record of previous experiment (5 marks)	Execution of experiment (5 marks)	Viva-Voce (5 marks)	Total (15 marks)	Remarks by Faculty
1	(i) Amplitude modulation and demodulation (ii) Spectrum analysis of AM	07-01-2020	3	2	2	7	Improve on Viva and revise experiments
2	(i) Frequency modulation and demodulation (ii) Spectrum analysis of FM		3	2	2	7	Improve on Viva and revise experiments
3	DSB-SC Modulator & Detector	07-01-2020	3	2	2	7	Improve on Viva and revise experiments
4	SSB-SC Modulator & Detector (Phase Shift Method)		3	2	2	7	Improve on Viva and revise experiments
5	Frequency Division Multiplexing & De multiplexing	21-01-2020	2	2	2	6	Improve on Viva and revise experiments
6	Pulse Amplitude Modulation & Demodulation	21-01-2020	3	2	2	7	Improve on Viva and revise experiments
7	Pulse Width Modulation & Demodulation	21-01-2020	3	2	2	7	Improve on Viva and revise

							experiments
8	Pulse Position Modulation & Demodulation	28-01-2020	3	2	2	7	Improve on Viva and revise experiments
9	Delta Modulation	18-02-2020	2	2	2	6	Improve on Viva and revise experiments
10	Frequency Shift Keying: Generation and Detection	25-02-2020	3	2	2	7	Improve on Viva and revise experiments
11	Binary Phase Shift Keying: Generation and Detection	18-02-2020	3	2	2	7	Improve on Viva and revise experiments
12	Generation and Detection (i) DPSK (ii) QPSK	25-02-2020	3	2	2	7	Improve on Viva and revise experiments
	Average					7	Improve on Viva and revise experiments

Faculty Member

HOD

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CHILKUR (V), MOINABAD, R.R. DIST-501 504

KG REDDY College of Engineering & Technology

DEPARTMENT

OF

ELECTRONICS AND COMMUNICATION ENGINEERING

NAME OF THE LABORATORY	**:**	**IC APPLICATIONS LAB**
YEAR AND SEM	**:**	**II B.TECH II SEM**
REGULATION/LAB CODE	**:**	**R18/ EC407PC**

IC APPLICATIONS LABORATORY MANUAL

HOD **PRINCIPAL**

KG REDDY College of Engineering & Technology

DEPARTMENT VISION

To be recognized as a full-fledged center for learning and research in various fields of Electronics and Communication Engineering through industrial collaboration and to provide consultancy for solving the real time socio-economic problems.

DEPARTMENT MISSION

- To provide innovative teaching and learning in the contemporary technologies in Electronics and Communication Engineering to support the professional aspirations of the students.
- To promote innovation through research and development among faculty and students by providing opportunities for inter-disciplinary learning in collaboration with industry.
- To encourage professional development of students that will inculcate ethical values and leadership skills while working with the community to address societal issues.

KG REDDY College of Engineering & Technology

Program Outcomes(PO's):

A graduate of the Electronics and Communication Engineering Program will demonstrate:

PO1: **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2: **Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6: **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: **Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one"s own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: **Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Educational Objectives (PEO's):

- **PEO 1:** To be equipped with skills for solving complex real-world problems related to VLSI, Embedded Systems, Signal/Image processing, and Digital and Wireless Communication.
- **PEO 2:** To develop professional skills that will equip them to succeed in their careers and encourage lifelong learning in advanced areas of Electronics and communications and related fields.
- **PEO 3:** To communicate effectively, work collaboratively and exhibit high levels of professionalism, moral and ethical responsibility.
- **PEO 4:** To develop the ability to understand and analyze engineering issues in a broader perspective with ethical responsibility towards sustainable development.

Program Specific Outcomes(PSO's)

- **PSO 1: Problem Solving Skills –** Graduates will be able to apply their knowledge in emerging electronics and communication engineering techniques to design solutions and solve complex engineering problems.
- **PSO 2: Professional Skills –** Graduate will be able to think critically, communicate effectively, and collaborate in teams through participation in co and extra-curricular activities.
- **PSO 3: Successful Career –** Graduates will possess a solid foundation in Electronics and Communications engineering that will enable them to grow in their profession and pursue lifelong learning through post-graduation and professional development.
- **PSO 4: Society Impact –** Graduate will be able to work with the community and collaborate to develop technological solutions that would promote sustainable development in the society.

SYLLABUS

IC APPLICATIONS LAB

B.Tech. III Year I Sem. **L T P C**

Course Code: EC407PC **0 0 3 1.5**

Note:

- Verify the functionality of the IC in the given application.

Design and Implementation of:

1. Inverting and Non-inverting Amplifiers using Op Amps.
2. Adder and Subtractor using Op Amp.
3. Comparators using Op Amp.
4. Integrator Circuit using IC 741.
5. Differentiator circuit using Op Amp.
6. Active Filter Applications – LPF, HPF (first order)
7. IC 741 Waveform Generators – Sine, Square wave and Triangular waves.
8. Mono-stable Multivibrator using IC 555.
9. Astable Multivibrator using IC 555.
10. Schmitt Trigger Circuits – using IC 741.
11. IC 565 – PLL Applications.
12. Voltage Regulator using IC 723.
13. Three Terminal Voltage Regulators –7805, 7809, 7912.

Course Outcomes (CO's)

Upon completion of this course, the student will be able to:

CO1: Design and perform op-amp 741 applications.
CO2: Calculate Duration of pulse widths generated in various multivibrators of timer IC555
CO3: Test and measure the locking and capturing of IC 565 PLL operation.
CO4. Perform Load and Line voltage Regulation on IC 723, Three terminal voltage regulators

INTRODUCTION TO THE INTEGRATED CIRCUIT APPLICATIONS LAB

Op-amp IC 741:-The short form of the operational amplifier is op-amp, is a one kind of solid state IC. The first operational amplifier is designed by Fairchild Semiconductors in the year 1963. It is the basic building block of analog electronic circuits that accomplish a different types of analog signal processing tasks. These ICs uses an exterior feedback to regulate its functions and these components are used as a multipurpose device in various electronic instruments. It consists of two inputs an two outputs, namely inverting and non inverting terminals, this 741 IC is most commonly used in various electrical and electronic circuits. The main intention of this 741 op amp is to strengthen AC & DC signals and for mathematical operations. The applications of operational amplifier mainly involve in filters, comparators, pulse generators, oscillators.

IC 555 Timer :-The 555 timer IC is an integral part of electronics projects. Be it a simple project involving a single 8 bit micro-controller and some peripherals or a complex one involving system on chips (SoCs), 555 timer working is involved. These provide time delays, as an oscillator and as a flip-flop element among other applications. The various applications includes Multivibrators, schmittrigger.

IC 565 PLL:-The PLL IC 565 is usable over the frequency range 0.1 Hz to 500 kHz. It has highly stable centre frequency and is able to achieve a very linear FM detection. The output of VCO is capable of producing TTL compatible square wave. The dual supply is in the range of ±6V to ±12V. The IC can also be operated from single supply in the range 12V to 24V.

IC 723 Voltage Regulator:-It consists of a voltage reference source , an error amplifier with its inverting input on pin 4 and non-inverting input on pin 5, a series pass transistor , and a current limiting transistor on pins 2 and 3. The device can be set to work as both posistive and negaive voltage regulators with an output voltage ranging from 2 V to 37 V, and output current levels up to 150 m A. The maximum supply voltage is 40 V, and the line and load regulations are each specified as 0.01%.

CONTENTS

EXPERIMENT.1

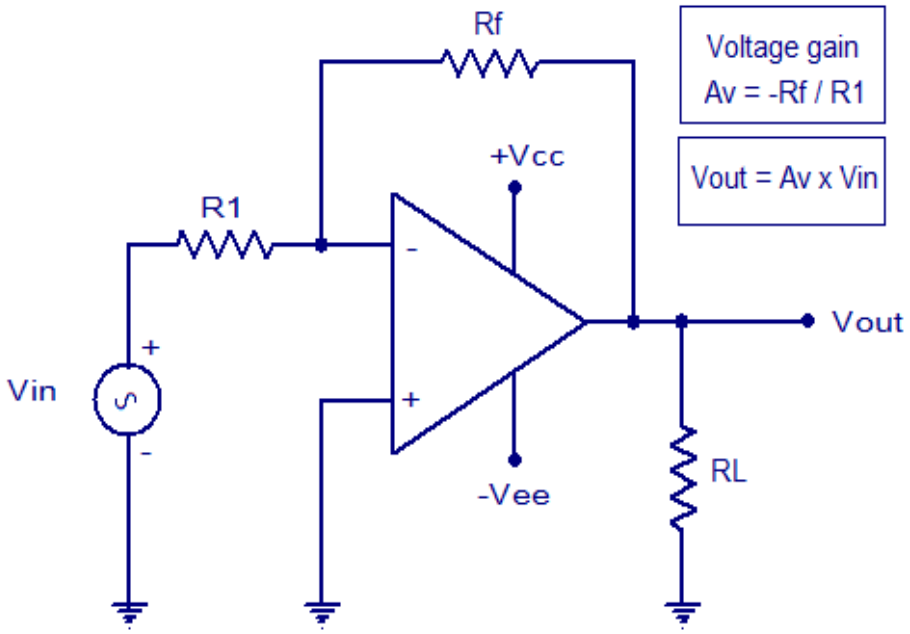
INVERTING AND NON-INVERTING AMPLIFIERS USING OP AMPS

AIM: Design and realize Inverting and Non-inverting amplifier using 741 Op-amp.

Apparatus Required: CRO, Function Generator, Bread Board, 741 IC, ±12V supply, Resistors 1KΩ, 10KΩ, and connecting leads.

Theory:

An inverting amplifier using opamp is a type of amplifier using opamp where the output waveform will be phase opposite to the input waveform. The input waveform will be amplifier by the factor Av (voltage gain of the amplifier) in magnitude and its phase will be inverted. In the inverting amplifier circuit the signal to be amplified is applied to the inverting input of the opamp through the input resistance R1. Rf is the feedback resistor. Rf and Rin together determine the gain of the amplifier. Inverting operational amplifier gain can be expressed using the equation Av = – Rf/R1. Negative sign implies that the output signal is negated. The circuit diagram of a basic inverting amplifier using opamp is shown below.



opamp inverting amplifier

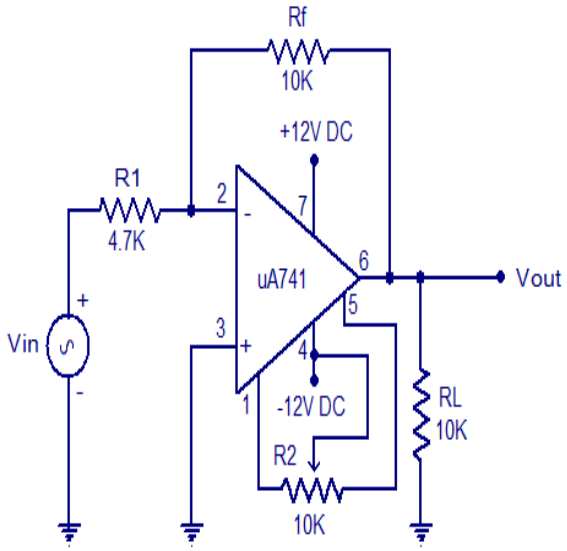
The input and output waveforms of an inverting amplifier using opamp is shown below. The graph is drawn assuming that the gain (Av) of the amplifier is 2 and the input signal is a sine wave. It is clear from the graph that the output is twice in magnitude when compared to the input (Vout = Av x Vin) and phase opposite to the input.

Practical inverting amplifier using 741.

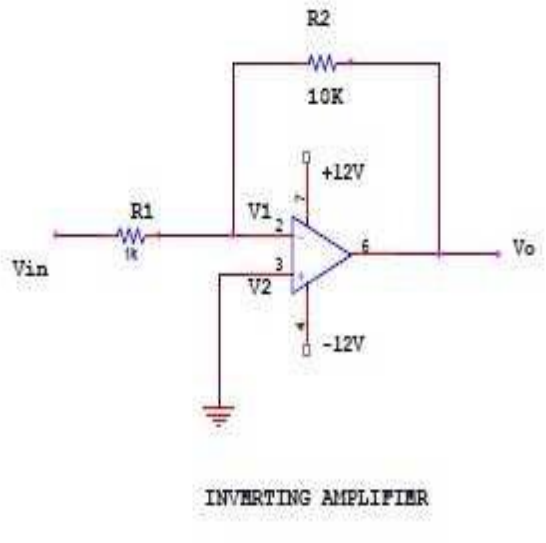
A simple practical inverting amplifier using 741 IC is shown below. uA 741 is a high performance and of course the most popular operational amplifier. It can be used in a verity of applications like integrator,

differentiator, voltage follower, amplifier etc. uA 741 has a wide supply voltage range (+/-22V DC) and has a high open loop gain. The IC has an integrated compensation network for improving stability and has short circuit protection. Signal to be amplified is applied to the inverting pi (pin2) of the IC. Non inverting pin (pin3) is connected to ground. R1 is the input resistor and Rf is the feedback resistor. Rf and R1 together sets the gain of the amplifier. With the used values of R1 and Rf the gain will be 10 (Av = -Rf/R1 = 10K/1K = 10). RL is the load resistor and the amplified signal will be

available across it. POT R2 can be used for nullifying the output offset voltage. If you are planning to assemble the circuit, the power supply must be well regulated and filtered. Noise from the power supply can adversely affect the performance of the circuit. When assembling on PCB it is recommended to mount the IC on the board using an IC base.



opamp inverting amplifier



INVERTING AMPLIFIER

In the inverting amplifier only one input is applied and that is to the inverting input (V2) terminal. The Non inverting input terminal (V1) is grounded.

Since, V1=0 V& V2=Vin

Vo= -A Vin

The negative sign indicates the output voltage is 1800 out of phase with respect to the input and amplified by gain A.

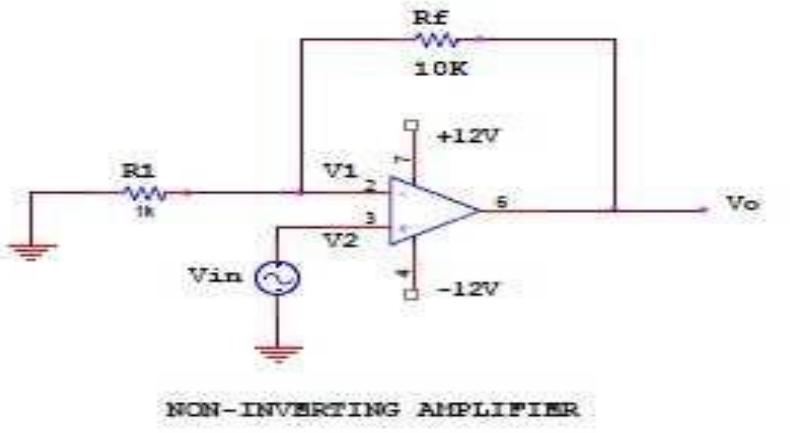
Practical Non-inverting amplifier using 741:

The input is applied to the non-inverting input terminal and the Inverting terminal is connected to the ground.

V1= Vin & V2=0 Volts

Vo= A Vin

The output voltage is larger than the input voltage by gain A & is in phase with the input signal.

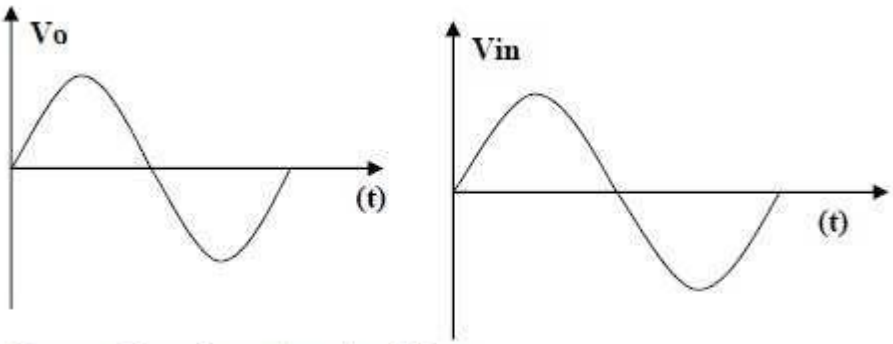


NON-INVERTING AMPLIFIER

Procedure:

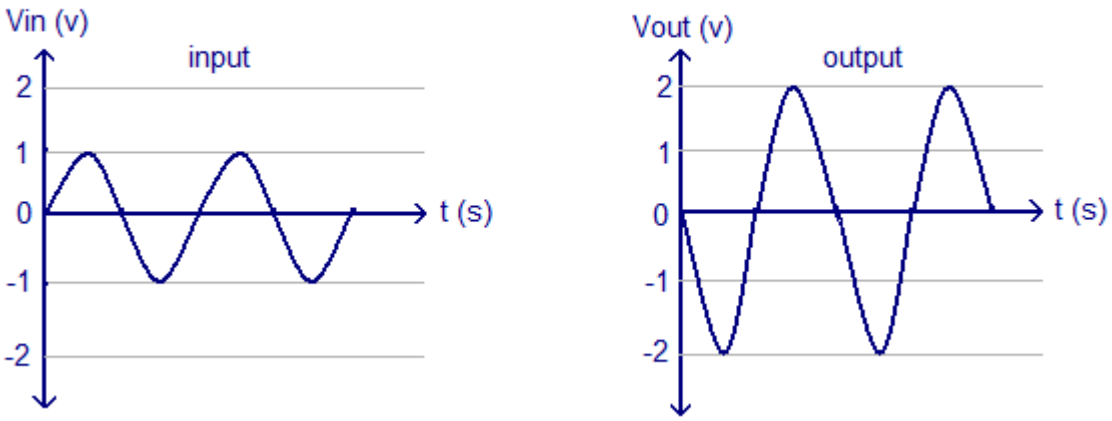
1) Connect the circuit for inverting, non inverting amplifier on a breadboard.
2) Connect the input terminal of the op-amp to function generator and output terminal to CRO.
3) Feed input from function generator and observe the output on CRO.
4) Draw the input and output waveforms on graph paper.

Output Waveform:



Output: Non- Inverting Amplifier

Input and output waveforms of an opamp inverting amplifier (gain assumed to be 2)



RESULT: Hence verified and drawn the operation and respective waveforms of inverting and non-inverting amplifier**.**

VIVA VOICE QUESTIONS:

1. Define an integrated circuit and classify them.
2. What is an op-amp and what are its types?
3. How to define the symbol of op-amp?
4. What are the various terminals of op-amp 741 IC?
5. What is the operating voltage range of IC 741?

EXPERIMENT.2

ADDER AND SUBTRACTOR USING OP AMP.

AIM:

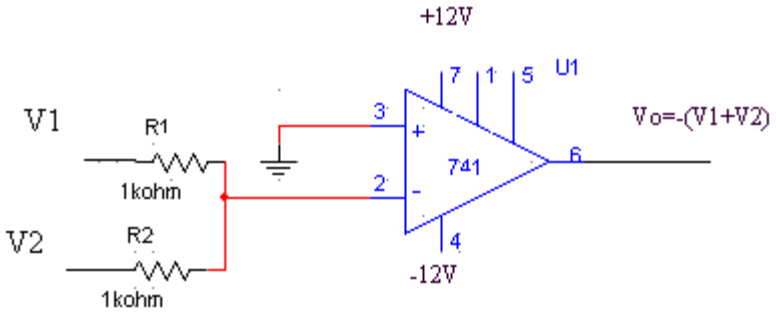
To study the applications of IC 741 as adder, subtractor.

APPARATUS:

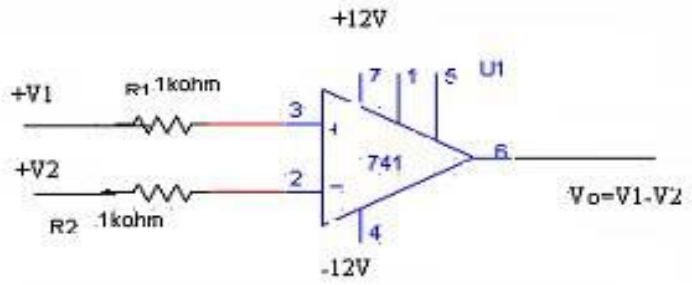
1. IC 741
2. Resistors (1KΩ)—4
3. Function generator
4. Regulated power supply
5. IC bread board trainer
6. CRO
7. Patch cards and CRO probes

CIRCUIT DIAGRAM

Adder:



Subtractor:



THEORY:

ADDER:

Op-Amp may be used to design a circuit whose output is the sum of several input signalssuchascircuitiscalledasummingamplifierorsummer.Wecanobtaineither inverting or non-inverting summer.

Thecircuitdiagramsshowsatwoinputinvertingsummingamplifier.Ithastwo input voltages $V_1$and V_2, two input resistors R_1, R2and a feedback resistor R_f.

Assumingthatopampisinidealconditionsandinputbiascurrentisassumedtobezero,there is no voltage drop across the resistor $R_{comp}$and hence then on inverting input terminal is at ground potential.
By taking nodal equations.

$V_1/R_1+V_2/R_2+V_0/R_f=0$
$V_0=-[(R_f/R_1)\ V_1+(R_f/R_2)\ V_2]$
And here $R_1=R_2=R_f=1K\Omega$
$V_0=-(V_1+V_2)$
Thus output is inverted and sum of input.

SUBTRACTOR:

A basic differential amplifier can be used as a subtractor. It has two input signals V1and V2and two input resistances R1andR2 and a feedback resistor R_f.The input signals scaled to the desired values by selecting appropriate values for the external resistors.

From the figure, the output voltage of the differential amplifier with a gain of'1' is
$V_0=-R/R_f(V_2-V_1)$
$V_0=V_1-V_2$.
Also $R_1=R_2=R_f=1K\Omega$.

Thus, the output voltage V_0 is equal to the voltage V_1 applied to then on inverting terminal minus voltage V_2applied to inverting terminal. Hence the circuit is subtractor.

OBSERVATIONS:
ADDER:

V_1(volts)	V_2(volts)	Theoretical $V_0=-(V_1+V_2)$	Practical $V_0=-(V_1+V_2)$

SUBTRACTOR:

V_1(volts)	V_2(volts)	Theoretical $V_0=(V_1-V_2)$	Practical $V_0=(V_1-V_2)$

PROCEDURE:

ADDER:

1. connections are made as per the circuit diagram.
2. Apply input voltage1) V_1=5v,V_2=2v
   2) V_1=5v,V_2=5v
   3) V_1=5v,V_2=7v.
3. Using Millimeter measure the dc output voltage at the output terminal.
4. For different values of $V_1$and V_2measure the output voltage.

SUBTRACTOR:

1. Connections are made as per the circuit diagram.
2. Apply input voltage1) V_1=5v,V_2=2v
   2) V_1=5v,V_2=5v
   3) V_1=5v,V_2=7v.
3. Using multi meter measure the dc output voltage at the output terminal.
4. For different values of $V_1$and V_2measure the output voltage.

PRECAUTIONS:

1. Make null adjustment before applying the input signal.
2. Maintain proper Vcc levels.

RESULT: Performed and tabulated the addition and subtraction operation on IC 741 op-amp.

VIVA-VOICE QUESTIONS:

1. What are an adder and subtractor?
2. Write the formulae for sum of three inputs for an op-amp.
3. What are the various DC characteristics of op-amp?
4. What are the various AC characteristics of op-amp?

EXPERIMENT.3

COMPARATORS USING OP AMP.

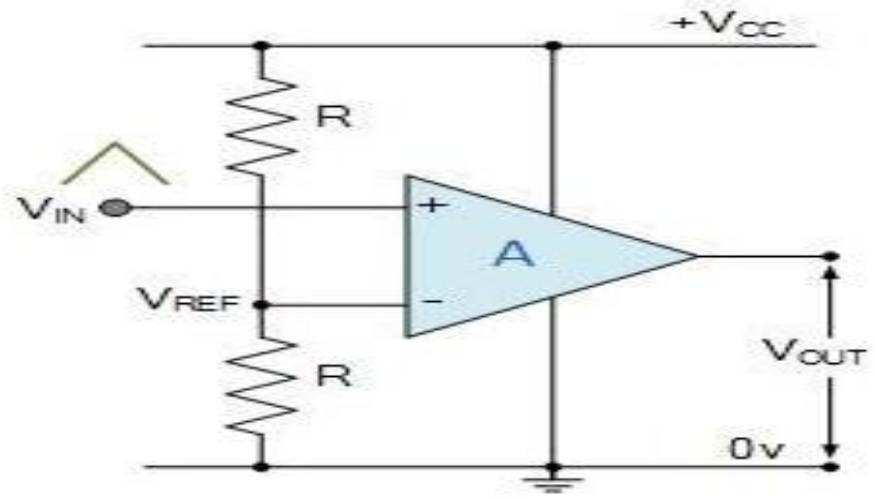
AIM:

To study the applications of IC 741 as comparator.

APPARATUS:

1. IC 741
2. Resistors (1KΩ)—4
3. Function generator
4. Regulated power supply
5. IC bread board trainer
6. CRO
7. Patch cards and CRO probes

CIRCUIT DIAGRAM



THEORY:

COMPARATOR:

A comparator is a circuit which compares a signal voltage applied atoneinputofanop-ampwithaknownreferencevoltageattheotherinput.Itisbasicallyanopen loop op-amp with output ±Vsat as in the ideal transfer characteristics.

It is clear that the change in the output state takes place with an increment in input Vi of only2mv.Thisistheuncertaintyregionwhereoutputcannotbedirectly defined. There are basically 2 types of comparators.

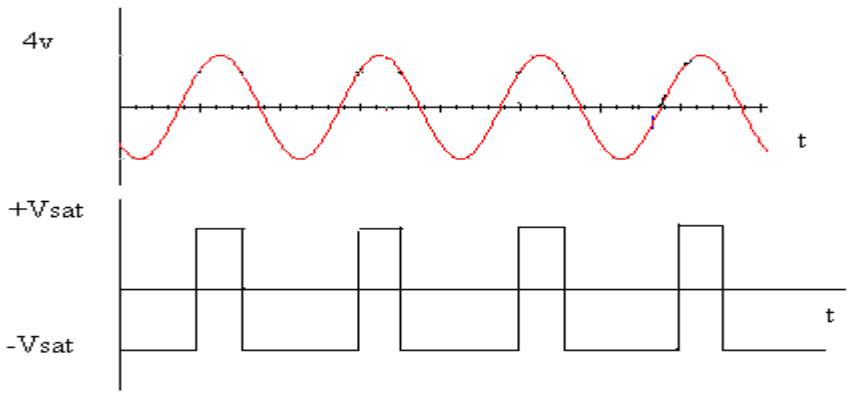
1. Non inverting comparator and.
2. Inverting comparator.

The applications of comparator are zero crossing detector, window detector, time marker generator and phase meter.

OBSERVATIONS:

Voltage input	V_{ref}	Observed square

MODEL GRAPH:



PROCEDURE:

1. Connections are made as per the circuit diagram.

2. Select the sine wave of10V peak to peak ,1K Hz frequency.
3. Apply the reference voltage 2V and trace the input and output wave forms.
4. Superimpose input and output waveforms and measure sine wave amplitude with reference to $V_{ref.}$
5. Repeat steps3and 4with reference voltages as 2V,4V,-2V,-4Vand observe the waveforms.
6. Replace sine wave input with 5V dc voltage and V_{ref}=0V.
7 Observe dc voltage at output using CRO.
8. Slowly increase V_{ref}voltage and observe the change in saturation voltage.

PRECAUTIONS:

1. Make null adjustment before applying the input signal.
2. Maintain proper Vcc levels.

RESULT: Hence performed comparison of time varying signal with a known reference voltage and drawn graphs

VIVA-VOICE QUESTIONS:

1. What is a comparator?
2. What is reference voltage?
3. Classify comparators?

EXPERIMENT.4

INTEGRATOR CIRCUIT USING IC 741

AIM:

To design and test an op-amp integrator

EQUIPMENTSANDCOMPONENTS:

APPARATUS

1. DC power supply	1 No.
2. CRO	1 No
3. BreadBoard	1No
4. FunctionGenerator-	1 No.

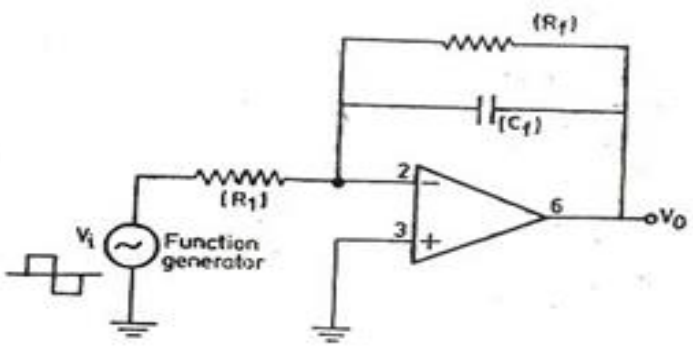
COMPONENTS:

1. 15 kΩ Resistor– 2 No.
2. 820 Resistor– 1 No.
3. 1.5 kΩ Resistor– 1 No.
4. 0.01 F Capacitor-2No
5. 0.5nF Capacitor-1No
6. IC741 - 1 No.

THEORY

The operational amplifier can be used in many applications. It can be used as differentiator and integrator. In integrator the circuit performs the mathematical operation of integration that is the output wave form is the integrative of the input waveform or good integration, one must ensure that the time period of the input signal is smaller than or equal to RfC1.the practical integrator eliminates the problem of instability and high frequency noise.

CIRCUITDIAGRAM:



PROCEDURE:

1. connect the integrator circuit as shown in fig.adjust the signal generator to produce a 5 volt peak sine wave at100 Hz.
2. observe input Vi and Vo simultaneously on the oscilloscope measure and record the peak value of Vo and the phase angle of Vo with respect to Vi.
3. Repeat step2 while increasing the frequency of the input signal. Find the maximum frequency at which circuit offers differentiation. Compare it with the calculated value of f_a Observe & sketch the input and output for square wave.
4. Connect the integrator circuit shown in Fig2.Set the function generator to produce a square wave of 1V peak-to-peak amplitude at 500Hz.View simultaneously output $V_o$and V_i.
5. Slowly adjust the input frequency until the output is good triangular waveform. Measure the amplitude and frequency of the input and output waveforms.
6. Verify the following relationship between R_1C_f and input frequency for good integration $f>f_a$ & $T<R_1C_1$ Where R_1C_f is the time constant
7. Now set the function generator to a sine wave of 1V peak-to-peak and frequency 500Hz. adjust the frequency of the input until the output is a negative going cosine wave. Measure the frequency and amplitude of the input and output waveforms.

OBSERVATIONS:

1. The time period and amplitude of the output waveform of differentiator circuit
2. The time period and amplitude of the integrator waveform

CALCULATIONS:

Integrator: Design an integrator that integrates a signal whose frequencies are between1 KHz and10 KHz.

$$f_b = \frac{1}{2R_1C_f}$$

The frequency at which the gain is 0 dB.

$$f_a = \frac{1}{2R_fC_f}$$

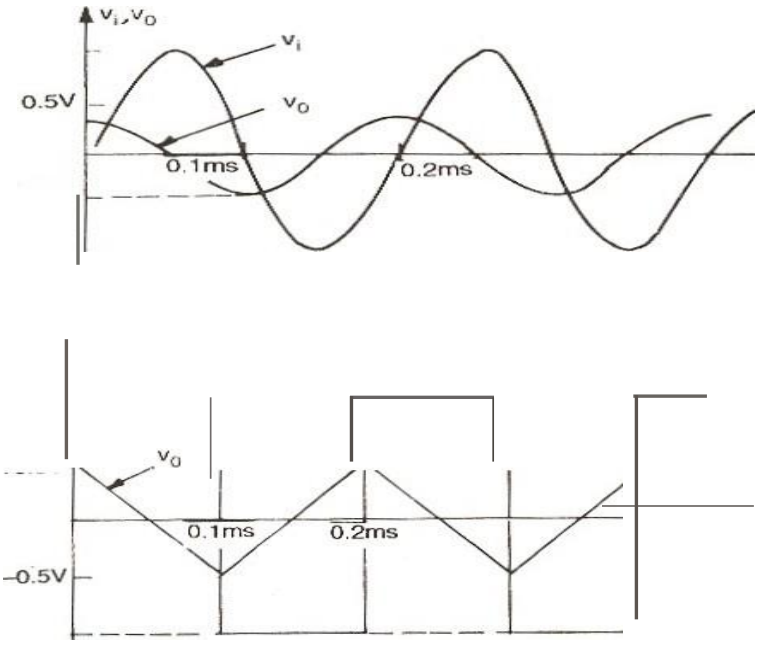
f_a: Gain limiting frequency,

The circuit acts as integrator for frequencies between $f_a$and f_b Generally $f_a<f_b$ [Ref. Frequency response of the integrator] Therefore choose f_a=1KHz

F_b=10 KHz Let C_f=0.01 F Therefore R_1=1.59k Choose R_1=1.5 K R_f=15 K

GRAPH:

Integrator:



RESULT: Hence performed the integration operation of op-amp and calculated its frequency?

Integrator

$$f_a=\frac{1}{2R_fC_f}$$

T=_____

VIVA-VOICE QUESTIONS:

1. What is an integrator?
2. In which condition an RC circuit acts as an integrator?
3. Define cut-off frequency of an integrator?

EXPERIMENT.5

DIFFERENTIATOR CIRCUIT USING OP AMP

AIM:

To design and test an op-amp differentiator and integrator

EQUIPMENTSANDCOMPONENTS:

APPARATUS

1. DC power supply - 1 No.
2. CRO - 1 No.
3. BreadBoard - 1 No.
4. FunctionGenerator- 1 No.

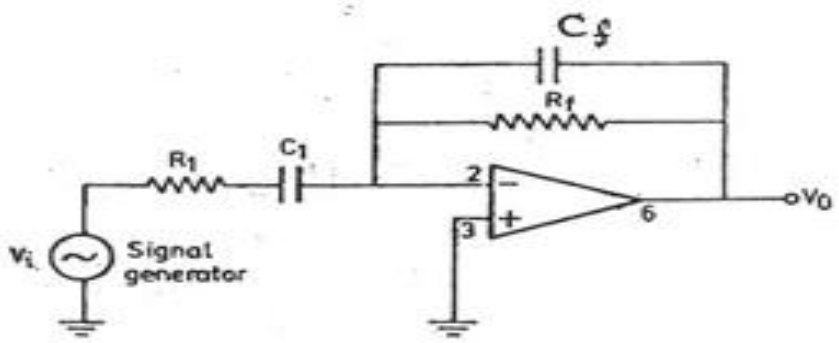
COMPONENTS:

1. 15 kΩ Resistor– 2 No.
2. 820 Resistor– 1 No.
3. 1.5 kΩ Resistor– 1 No.
4. 0.01 F Capacitor-2No
5. 0.5nF Capacitor-1No
6. IC741 - 1 No.

THEORY

The operational amplifier can be used in many applications. It can be used as differentiator and integrator. In differentiator the circuit performs the mathematical operation of differentiation that is the output wave form is the derivative of the input waveform or good differentiation, one must ensure tha the time period of the input signal is larger than or equal to RfC1.the practical differentiator eliminates the problem of instability and high frequency noise.

CIRCUITDIAGRAM:



PROCEDURE:

1. connect the differentiator circuit as shown in fig.adjust the signal generator to produce a 5 volt peak sine wave at100 Hz.
2. observe input Vi and Vo simultaneously on the oscilloscope measure and record the peak value of Vo and the phase angle of Vo with respect to Vi.
3. Repeat step2 while increasing the frequency of the input signal. Find the maximum frequency at which circuit offers differentiation. Compare it with the calculated value of f_a Observe & sketch the input and output for square wave.
4. Connect the integrator circuit shown in Fig2.Set the function generator to produce a square wave of 1V peak-to-peak amplitude at 500Hz.View simultaneously output $V_o$and V_i.
5. Slowly adjust the input frequency until the output is good triangular waveform. Measure the amplitude and frequency of the input and output waveforms.
6. Verify the following relationship between R_1C_f and input frequency for good integration $f>f_a$ & $T<R_1C_1$ Where R_1C_f is the time constant
7. Now set the function generator to a sinewave of 1V peak-to-peak and frequency 500Hz. Adjust the frequency of the input until the output is a negative going cosine wave. Measure the frequency and amplitude of the input and output waveforms.

OBSERVATIONS:

1. The time period and amplitude of the output waveform of differentiator circuit
2. The time period and amplitude of the integrator waveform

CALCULATIONS:

Design a differentiator to differentiate an input signal that varies infrequency from10 Hz to 1 kHz.

$f = \frac{1}{2R_fC_1}$

f_a=1 kHz, the highest frequency of the input signal

Let C_1=0.01 F, Then

R_f=15.9 k

Therefore choose R_f=15.0 k

$f = \frac{1}{2R_1C_1}$

Choose: f_b=20x f_a=20 KHz

Hence R_1=795

Therefore choose R_1=820

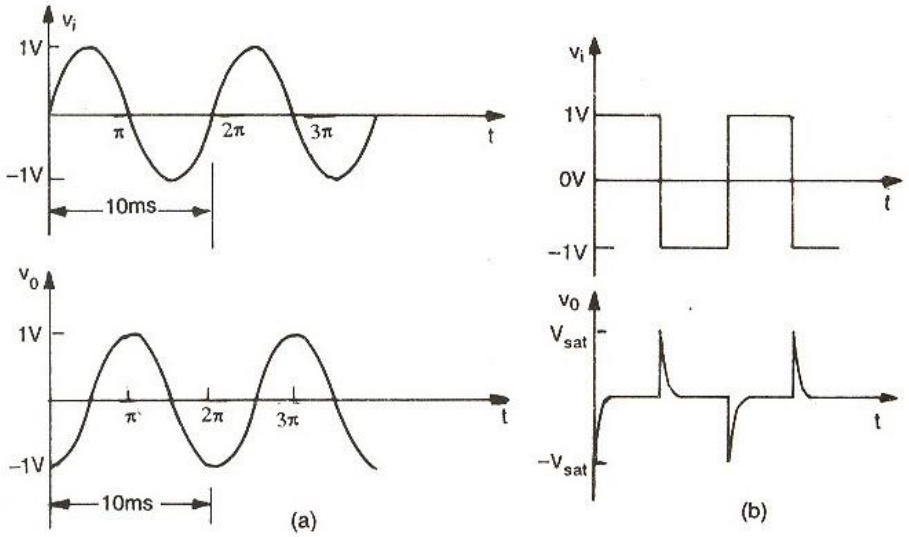
Since $R_1C_1=R_fC_f$ (compensated attenuator)

C_f=0.54 nF

Therefore choose C_f=0.5nF

GRAPH:

Differentiator



RESULT: Hence performed the integration operation of op-amp and calculated its frequency?

Differentiator

$f_b = \frac{1}{2R_1C_f}$

T>R_f C_1=_____

VIVA-VOICE QUESTIONS:

1. What is differentiator?
2. In which condition an RC circuit acts as differentiator?
3. Define cut-off frequency of differentiator?
4. Compare differentiator and integrator?

EXPERIMENT.6

ACTIVE FILTER APPLICATIONS-LPF, HPF [FIRSTORDER]

AIM:

To study Op-Amp as first order LPF and first order HPF and to obtain frequency response.

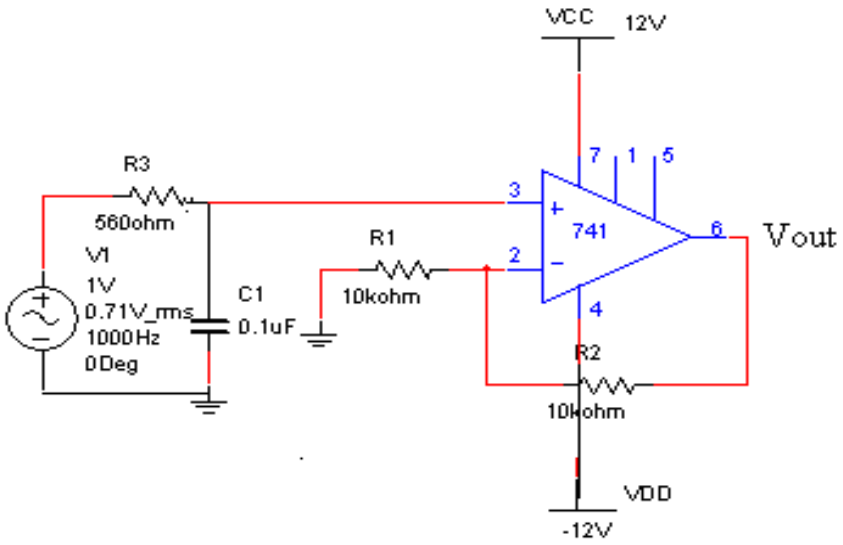
APPARATUS:

1. IC 741.
2. Resistors (10KΩ--2, 560Ω, 330Ω
3. Capacitors(0.1Ω)
4. Bread board trainer
5. CRO
6. Function generator
7. Connecting wires
8. Patch cards.

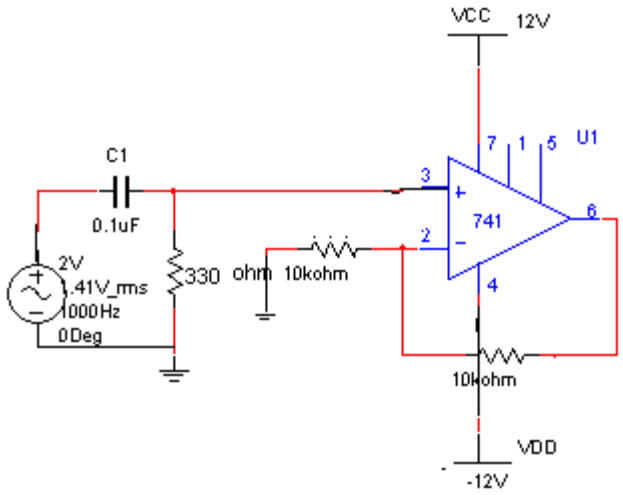
CIRCUIT

DIAGRAM: (a)

LPF



(a)HPF



THEORY: LOWPASS

FILTER:

The first order low pass butterworth filter uses an Rc network for filtering. The op-amp is used in then on inverting configuration, hence it does not load down the RC network. Resistor R1 and R2 determine the gain of the filter.

$V_0/Vin=A_f/(1+jf/f_h)$

A_f=1 +R_f/R_1=pass band gain of filter .
F=frequency of the input signal.
F_h= 1/2ΠRC =High cutoff frequency of filter .
V0/Vin =Gain of the filter as a function of frequency

The gain magnitude and phase angle equations of the LPF the can be obtained by converting V0/Vin into its equivalent polar form as follows

$|V_0/Vin|=A_f/(\sqrt{1+(f/f_l)^2})$

$\Phi = - \tan^{-1}(f/f_h)$

WhereΦisthephaseangleindegrees.TheoperationoftheLPFcanbeverified from the gain magnitude equation.

1. At very low frequencies i.e $f<f_h$,
   $|V_0/Vin|=A_f$.
2. At $f=f_h$,$|V0/Vin|=A_f/\sqrt{2}$.
3. At $f>f_h$,$|V0/Vin|<A_f$.

HIGH PASS FILTER:

High pass filters are often formed simply by interchanging frequency. Determining resistors and capacitors in LPFs that is, a firstorder HPF is formed froma firstorderLPFbyinterchangingcomponents'R'and'C'figure.Showsafirstorder butterworth HpF with a lower cutoff frequency of 'Fl'. This is the frequency at which magnitude of the gain is 0.707times its pass band value. Obviously all frequencies, with the highest frequency determinate by the closed loop band width of op-amp.

For the first order HPF ,the output voltage is

$$V0 =[1+ R_f/R_1]\ j2\Pi RCVin/(1- j2\Pi fRC)$$

$V_0/Vin=A_f[j(f/f_l)/(1=j(f/f_l)]$

Where A_f+ R_f/R_1a pass band gain of the filter.

F=frequency of input signal.
$F_l=1/2\Pi RC$ = lower cutt off frequency
Hence, the magnitude of the voltage gain is

$|V_0/Vin|=A_f(f/f_l)/\sqrt{1+(f/f1)^2}$.

Since, HPFs are formed from LPFs simply by interchanging R'sandC's. The design and frequency scaling procedures of the LPFs are also applicable to HPFs.

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Apply sine wave of amplitude $4V_{p-p}$ to the non inverting input terminal.
3. Values the input signal frequency.
4. Note down the corresponding output voltage.
5. Calculate gain in db.
6. Tabulate the values.
7. Plot a graph between frequency and gain.
8. Identify stop band and pass band from the graph.

OBSERVATIONS:

Low Pass Filter

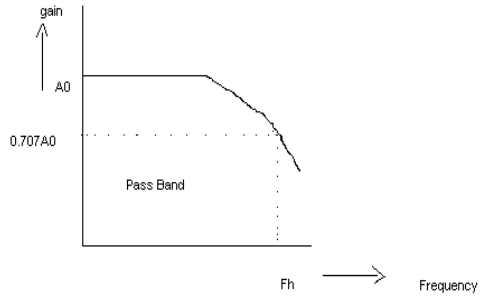
Frequency(Hz)	V0(V)	Gain in db= 20log(V0/Vi)

High Pass Filter

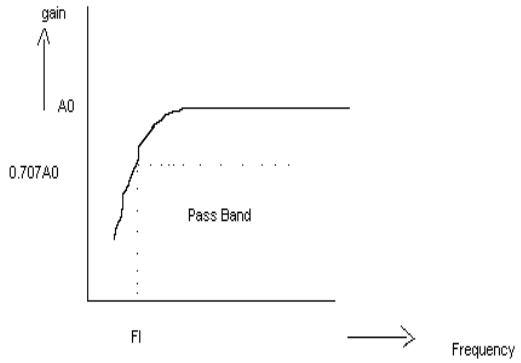
Frequency(Hz)	V0(V)	Gain in db= 20log(V0/Vi)

MODEL GRAPH:

High Pass Filter



Low Pass Filter



PRECAUTIONS:

1. Make null adjustment before applying the input signal.
2. Maintain proper Vcc levels.

RESULT: Performed filter operation of op-amp 741 and plotted the graph.

VIVA-VOICE QUESTIONS:

1. What is a filter circuit?
2. Classify various filters?
3. Calculate the cut-off frequency of low pass filter.
4. What is 3db frequency.

EXPERIMENT.7

IC 741 WAVEFORM GENERATORS – SINE, SQUARE WAVE AND TRIANGULAR WAVES.

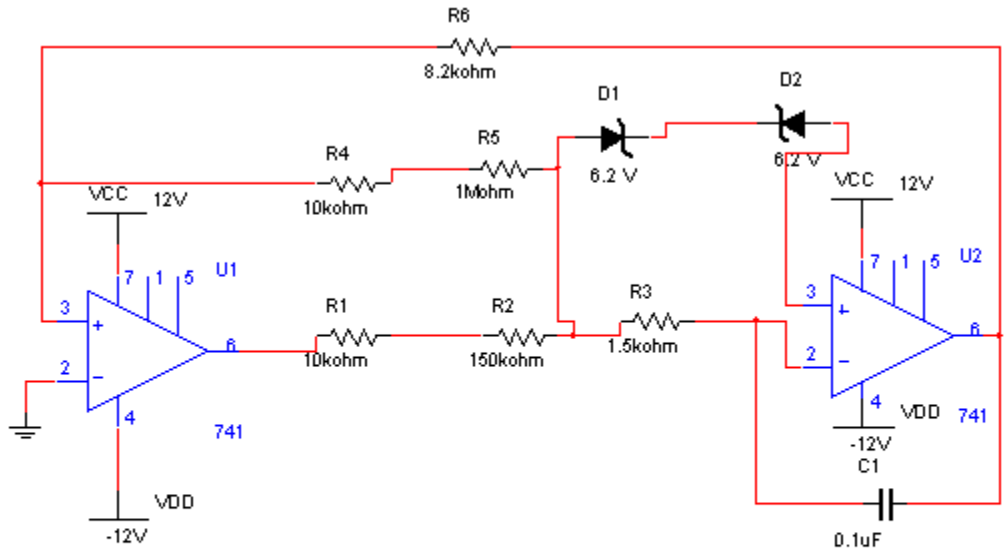
AIM:

To generate triangular and square waveforms and to determine the time period Of the waveforms.

APPARATUS:

1. Op-Amp IC 741 –2 Nos
2. Bread board IC trainer
3. Capacitor 0.1µF
4. Zener diodes (6.2V)—2 Nos
5. Resistors—10KΩ, 150KΩ1.5KΩ, 1MΩ, 8.2KΩCRO
6. Patch cards
7. Connecting wires

CIRCUIT DIAGRAM:



THEORY:

The function generator consists of a comparator U1and an integrator A2.The comparator U2 compares the voltage at point P continuously with the inverting input i.e., atzerovolts.WhenvoltageatPgoesslightlybeloworabovezerovolts,theoutputof U1 is at the negative or positive saturation level, respectively.

To illustrate the circuit operation let us set the output of U1at positive saturation +Vsat(approximately +Vcc). This +Vsat is an input to the integrator U2.Theoutputof U2 ,therefore will be a negative going ramp. Thus, one end of the voltage divider R2-R3 is the positive saturation voltage +Vast of U1 and the other is the negative going ramp ofU2. When the negative going ramp attains a certain value–Vramp, point p is slightly below zero volts; hence the output of U1 will switch from positive saturation to negative saturation–Vsat (approximately–Vcc). This means that the output of U2 will now stop going negatively and will begin to go positively. The output of U2 will continue to increase until it reaches +Vramp. At this time the point P is slightly above zero volts. The sequence then repeats. The frequencies of the square are a function of the d.c supply voltage. Desired amplitude can be obtained by using approximate zeners at the output ofU1.

THEORETICAL VALUES:

Time period, $T=4R_5C\ (R_3+R_4)/(R_1+R_2) =0.492$ msec.
Positive peak ramp = $Vz\ R_5/(R_1+R_2) =0.05$ volts.

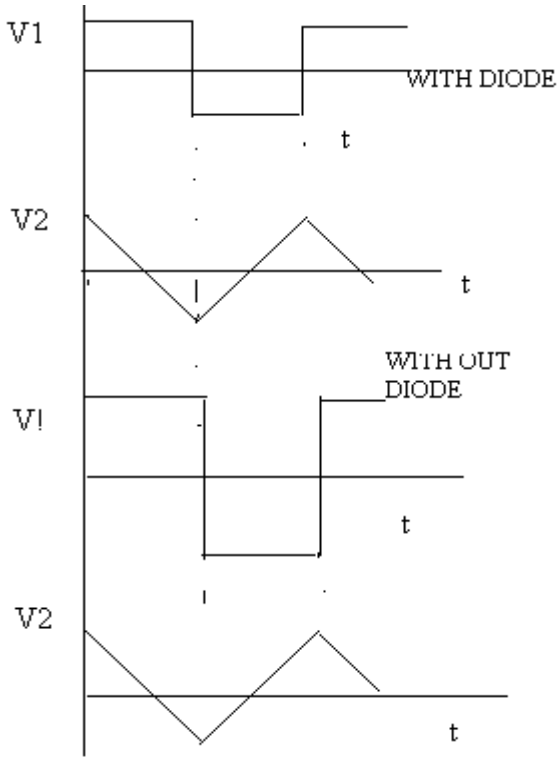
PRACTICAL VALUES:

Timeperiods of triangular wave= Time
periods of square wave= Positive peak
ramp=
Voltage of square wave=

PROCEDURE:

1. The circuit is connected as shown in the figure.
2. The output of the comparator U1 is connected to the CRO through chennal1,to generate a square wave.
3. The output of the comparator U2 is connected to the CRO through chennal2, to generate a triangular wave.
4. The time periods of the square wave and triangular waves are noted and they are found to be equal.

MODEL GRAPH:



PRECAUTIONS:

1. Make null adjustment before applying the input signal.
2. Maintain proper Vcc levels.

RESULT: Generated and plotted sine, square and triangular waveforms using op-amp.

VIVA-VOICE QUESTIONS:

1. **What are basic waveforms available?**
2. **Define sine wave?**
3. **Calculate the time period of square wave?**

EXPERIMENT.8

MONO-STABLE MULTIVIBRATOR USING IC 555.

AIM:

To construct and study the operation of a monostable multivibrator using555IC timer.

APPARATUS:

1. 555 IC timer
2. Capacitors (0.1µF,0.01µF)
3. Resistors 10KΩ
4. Bread board IC trainer
5. CRO
6. Connecting wires and Patch cards

THEORY:

Monostable multivibrator is also known as triangular wave generator. It has one stable and one quasi stable state. The circuit is useful for generating single output pulse of time duration in response to a triggering signal. The width of the output pulse depends only on external components connected to the op-amp. The diode gives a negative triggering pulse. When the output is +Vsat, a diode clamps the capacitor voltage to 0.7V. Then, a negative going triggering impulse magnitude Vi passing through RC and the negative triggering pulse is applied to the positive terminal.

Let us assume that the circuit is in stable state. The output V0 is at +Vsat. The diode D1conducts and Vc the voltage across the capacitor 'C' gets clamped to 0.7V .the voltage at the positive input terminal through R1 R2 potentiometer divider is +ß Vsat. Now, if a negative trigger of magnitude Vi is applied to the positive terminal so that the effective signal is less than 0.7V. the output of the Op-Amp will switch from +Vsat to– Vsat. The diode will now get reverse biased and the capacitor starts charging exponentially to–Vsat. When the capacitor charge Vc becomes slightly more negative than –ß Vsat, the output of the op-amp switches back to +Vsat. The capacitor 'C' now starts charging to +Vsat through R until Vc is 0.7V.

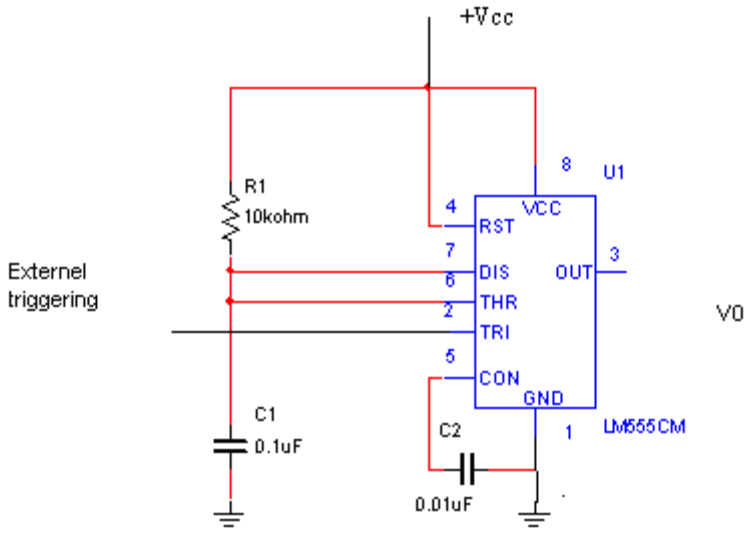
$$V_0 = V_f + (V_i - V_f)\, e^{-t/RC}.$$

$$ß = R_2/(R_1+R_2)$$

If $V_{sat} >> V_p$ and $R_1 = R_2$ and ß=0.5,

Then, T=0.69RC.

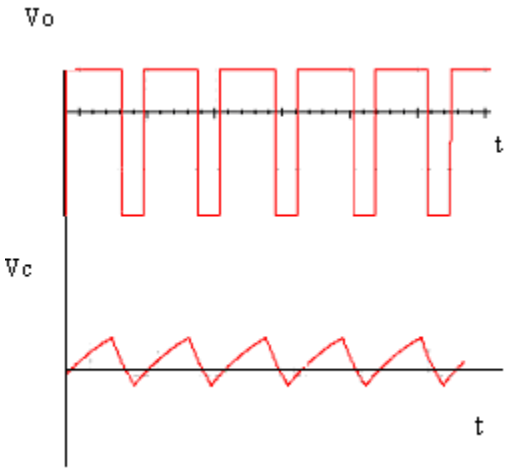
CIRCUIT DIAGRAM:



PROCEDURE:

1. Connections are made as per the circuit diagram.
2. Negative triggering is applied at the terminal 2.
3. The output voltage is measured by connecting the channel-1 at pin3.
4. Theoutputvoltageacrosscapacitorismeasuredbyconnectingthechannel-2at the point 'P'.
5. Theoretically the time period is calculated by $T=1.1R_1C_1$ where R_1 =10KΩ C_1=0.1μF.
6. Practically the charging and discharging timers are measured and theoretical Value of time period is measured with practical value

MODELGRAPH:



PRECAUTIONS:

1. Make the null adjustment before applying the input signal.
2. Maintain proper Vcc levels.

RESULT: Studied the operation of Monostable multivibrator using 555 timers.

VIVA-VOICE QUESTIONS:

1. What is multivibrator?
2. How the 555 given to the circuit.
3. What are the applications of Monostable multivibrator?
4. What is the pulse width of Monostable multivibrator?

EXPERIMENT.9

ASTABLE MULTIVIBRATOR USING IC 555

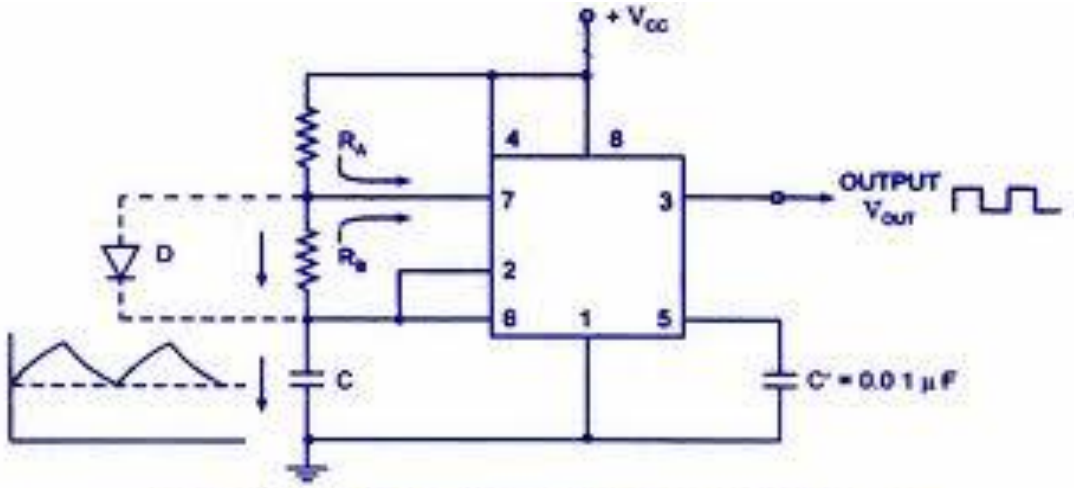
AIM:

To construct and study the operation of A stable multivibrator using 555 timer

APPARATUS:

1. IC 555 Timer
2. Resistors (10 KΩ,4.7 KΩ)
3. Diode (IN 4007)
4. Capacitors (0.1µF,0.01µF)
5. CRO
6. Patch cards
7. CRO Probes
8. Connecting wires

CIRCUIT DIAGRAM:



Circuit of The Timer 555 as an Astable Multivibrator

THEORY:

A simple OPAMP a stable multivibrator is also called square wave generator and free running oscillator .The principle for the generation of square wave output is to force an OP_AMP to operate in the saturation region β=R2/(R1+R2) of the output is feedback to input. The output is also feedback to the negative input terminal after integrating by means of a RCLPF whenever the negative input just exceeds Vref, switching takes place resulting in a square wave output. In a stable multivibrator both states are quasi stable states.

When the output is +Vsat, the capacitor is now starts charging towards +Vsat through resistance R the voltage is held at +βVsat. This condition continuous until the charge on C just exceed Vsat. Then the capacitor begins to dis charge towards– Vsat. Then the capacitor charges more and more negatively until its voltage just– βVsat. The frequency is determined by the time it takes the capacitor to charge from– β Vsat and +β Vsat

$$Vc(t)= Vf+(Vi-Vf)e^{-t/RC}$$

$$Vc(t)= Vsat-Vsat(1+\beta)e^{-t/RC}$$

We get $T1=RC \ln((1+\beta)/(1-\beta))$

$T=2T1=2 RC \ln ((1+\beta)/(1-\beta))$, $Vo(p-p)=2Vsat$

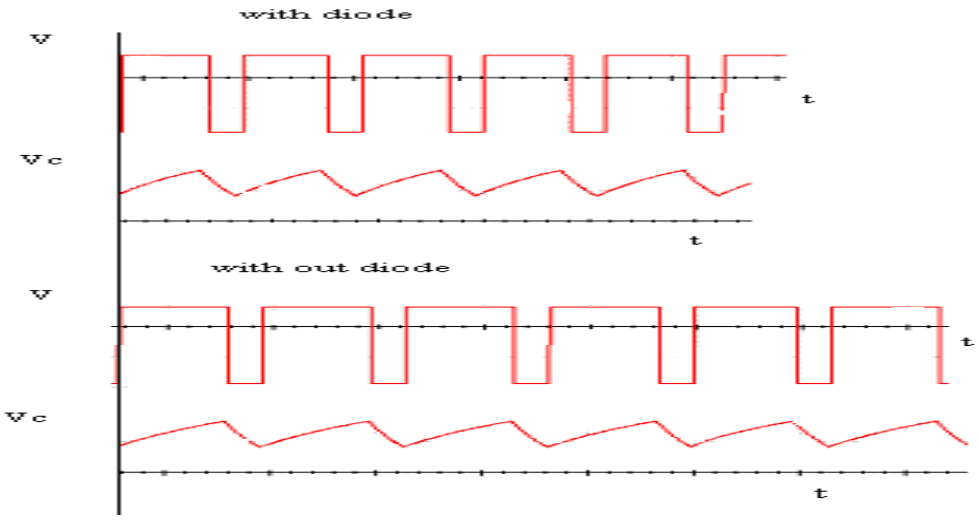
PROCEDURE:

1. Connections are made as per the circuit diagram.
2. .Pins 4 and 8 are shorted and connected to power supply Vcc (+5V)
3. Between pins 8 and 7 resistor R1 of10KΩ is connected and between 7 and 6 resistor R2 of 4.7KΩ is connected. Pins 2 and 6 short circuited.
4. In between pins 1 and 5 a Capacitor of0.01μF is connected.
5. The out put is connected across the pin 3 and GND.
6. In between pins 6 and GND a Capacitor of 0.1μF is connected.
7. Theoretically with out diode charging time Tc is given by
   Tc=0.69(R1+R2) C1,
   Discharging time Td is given by Td=0.69R2C1
   The frequency f is given by f=1.45/ (R1+2R2)C1
   %of Duty cycle is (Tc/ (Tc+Td))*100.
8. Practically Td and Tc are measured and wave forms are noted and theoretical Values are verified with practical values
9. Connect diode between pins 7 and 2.
10. Theoretically with diode connected charging time is given by Tc=0.69R1C1 Discharging time is given by Td=0.69R2C1
11. Practically Td and Tc are noted and verified with theoretical values

OBSERVATIONS:

With diode		without diode	
Theoretical	Practical	Theoretical	Practical

MODEL GRAPH:



PRECAUTIONS:

1.Make null adjustment before applying the input signal.
2.Maintain proper Vcc levels.

RESULT: Studied the operation of Monostable multivibrator using 555 timers.

VIVA-VOICE QUESTIONS:

1. What is an astable multivibrator?
2. How the 555 circuit acts as an astable multivibrator?
3. What are the applications of astable multivibrator?
4. What is the pulse width of astable multivibrator?

EXPERIMENT.10

SCHMIT TRIGGER CIRCUIT USING IC 741

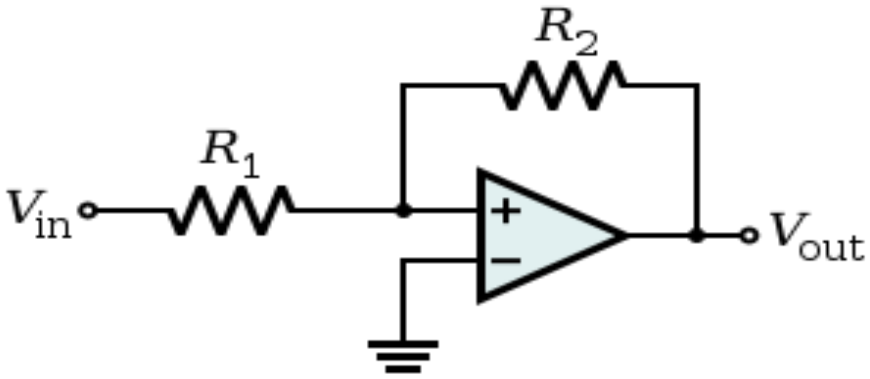
Aim:

To construct the Schmitt trigger using Ic 741

Apparatus:

5. 741 IC
6. Function Generator
7. Bread board
8. Resistors
9. Power supply
10. Connection wire

Circuit Diagram



PROCEDURE:

1.Connect the circuit as shown in the figure.
2.Apply the input sine wave at pin number 2 of IC 741.
3.Observe the square wave output at pin 6
4.Measure UTP and LTP and compare them with theoretical values.

PRECAUTIONS:

1.Loose connections should be avoided.
2.Switch on the supply after verification of the circuit
3.Waveforms and readings should be taken with out parrellax error.

RESULT: Hence designed and conducted experiment on 555 timer as a schmitttrigger.

VIVA-VOICE QUESTIONS:

1. What is schmitttrigger?
2. How it convets sine wave into rectangular?
3. Wgat is hysterisis?

EXPERIMENT.11

IC 565 PLL-APPLICATIONS

AIM:

1. To study the operation of NE565 PLL
2. To use NE565 as a multiplier

EQUIPMENTSANDCOMPONENTS:

APPARATUS		
1. DC power supply 2. CRO	- -	1 No. 1 No.
3. Bread Board	-	1 No.
4. Function	-	1 No.

COMPONENTS:

1. 6.8 kΩ Resistor– 1 No.
2. 0.1 F Capacitor– 1 No
5. 0.001 F Capacitor– 2 Nos
6. IC565 - 1 No.

THEORY:

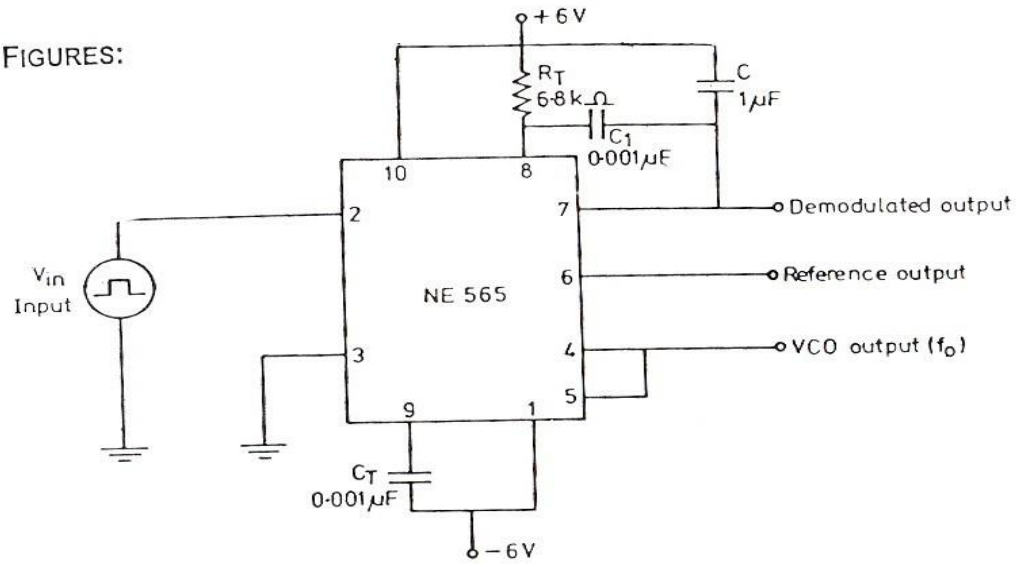
The 565 is available as a14-pin DI P package. It is produced by sign at c corporation. The output frequency of the VCO can be re written as

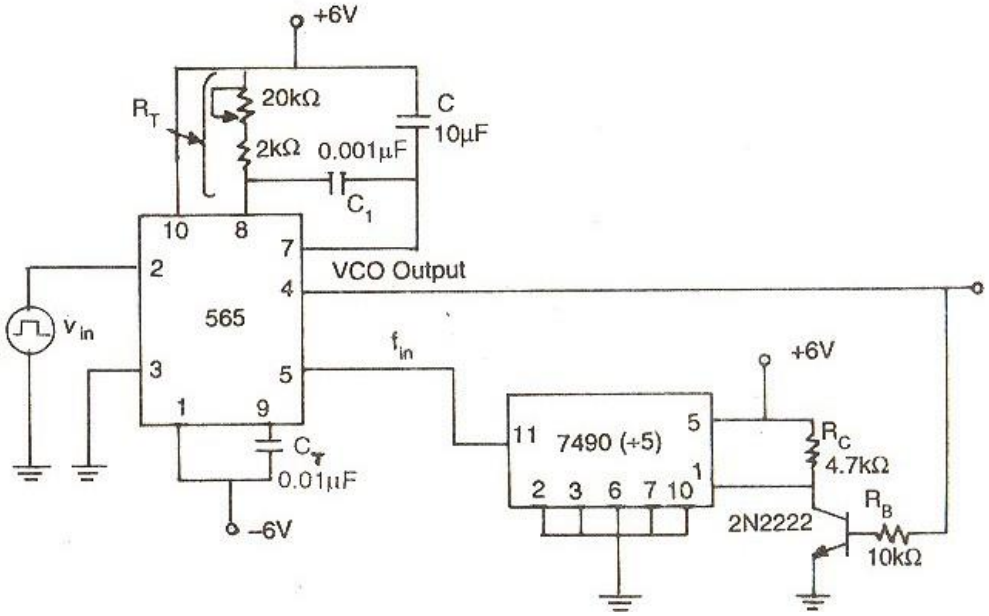
$$f_o = \frac{0.25}{R_T C_T} Hz$$

Where R_T and C_T are the external resistor and capacitor connected to pin8 and pin9. A value between 2k and 20k is recommended for R_T.The VCO free running frequency is adjusted with $R_T$and C_T to be at the centre for the input frequency range.

CIRCUITDIAGRAM:

FIGURES:





PROCEDURE:

i. Connect the circuit using the component values as shown in the figure

ii .Measure the free running frequency of VCO at pin4 with the input signal V_{in}set=zero. Compare it with the calculated value=$0.25/R_TC_T$

iii. Now apply the input signal of 1Vpp squarewaveata1kHz topin2

iv. Connect1 channel of the scope to pin2 and display this signal on the scope.

v . Gradually increase the input frequency till the PLL is locked to the input frequency. This frequency f_1 gives the lower ends of the capture range. Go on increase the input frequency, till PLL tracks the input signal, say to a frequency f_2.This frequency f_2 gives the upper end of the lock range. If the input frequency is increased further the loop will get unlocked.

vi. Now gradually decrease the input frequency till the PLL is a gain locked. This is the frequency f_3, the upper end of the capture range .Keep on decreasing the input frequency until the loop is unlocked. This frequency f_4 gives the lower end of the lock range

vii. The lock range $f_L=(f_2– f_4)$ compare it with the calculated value.

Also the capture range is $f_c=(f_3– f_1)$. Compare it with the calculated value of capture range.

viii. To use PLL as a multiplie5r,makeconnectionsas show in fig. The circuit uses a 4-bitbinarycounter7490 usedasadivide-by-5circuit.

ix.Settheinputsignalat1Vpp squarewaveat500Hz

x..Vary the VCO frequencybyadjustingthe20KpotentiometertillthePLLis locked. Measure the output frequency

xi. Repeatstep9 and10 for input frequency of 1kHzand1.5kHz.

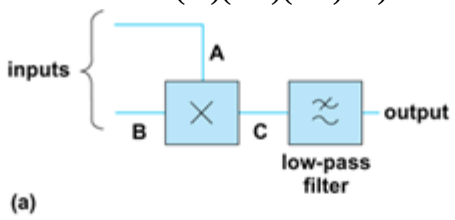
OBSERVATIONS:

fo =_____

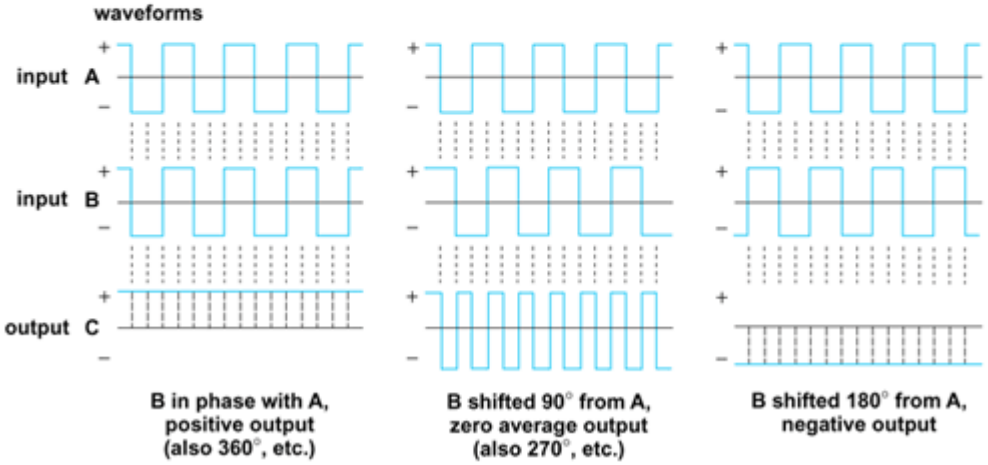
f_L=_____

f_C=_____

$$\frac{f_L}{(2\ )(3.6)(10^3)xC)^{1/2}}$$



(a)



RESULT: Hence observed the characteristics of PLL IC 565.

fo=_____

fL=_____

fC=_____

VIVA-VOICE QUESTIONS:

1. Define lock range?
2. Define capture range?
3. What are the applications of PLL.

EXPERIMENT.12

12. VOLTAGE REGULATORUSING IC 723

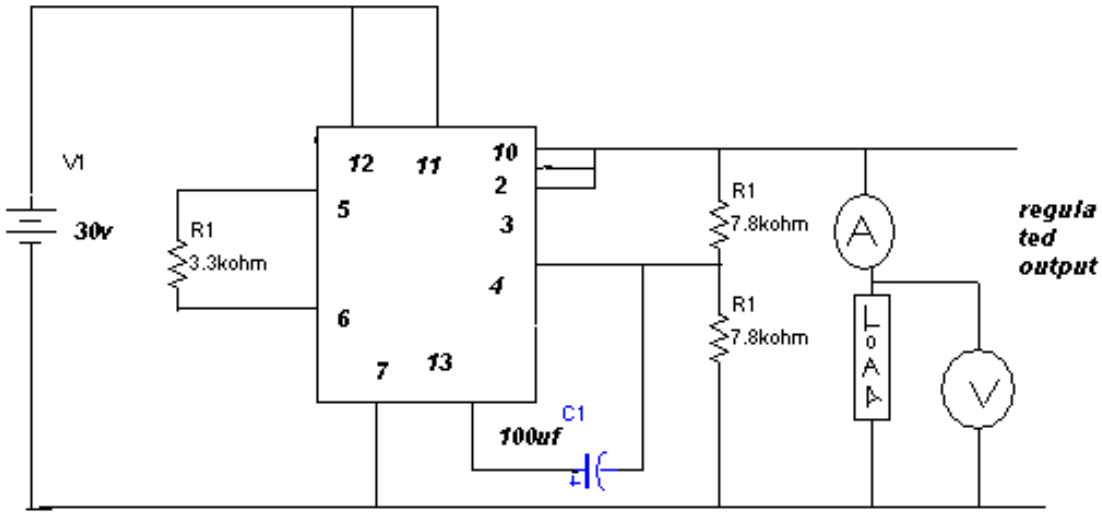
AIM:

To plot the regulation characteristics of the given IC LM 723.

APPARATUS:

1. Bread board
2. IC LM 723
3. Resistors(7.8KΩ ,3.9KΩ)
4. RPS
5. DRB
6. Capacitors 100µF
7. Patch cards
8. Connecting wires

CIRCUIT DIAGRAM:



THEORY:

A voltage regulator is a circuit that supplies constant voltage regardless of changes in load currents. Except for the switching regulators, all other types of regulators are called line arregulators.ICLM723is general purpose regulator. The input voltage ofthis 723ICi s40V maximum. Output voltage adjustable from 2Vto30
V. 150mA output current external pass transistor. Output currents in excess of 10Amperepossiblebyaddingexternaltransistors.Itcan be used as either a linear or a switching regulator. The variation of DC output voltage as a function of DC load current is called regulation.

% Regulation = [(Vnl-Vfl)/Vfl]*100

PROCEDURE:

(1).LINE REGULATION

1. Connections are made as per the circuit diagram
2 .Power supply is connected to12 and 7 terminals
3. Volt meter is connected to10 and 7 terminals
4. By increasing the input voltage corresponding volt meter reading is noted.

(2).LOAD REGULATION

1. Connect the load to the terminals 10 and GND.
2. Keep the input voltage constant at which line regulation is obtained
3. The maximum load value is calculated from IC ratings.
4. Now, we decrease the load resistance and note down the corresponding value of the output in volt meter.
5. Plot the graph for load verses load regulation.

OBSERVATIONS:

(1).LINEREGULATION: Vnl=

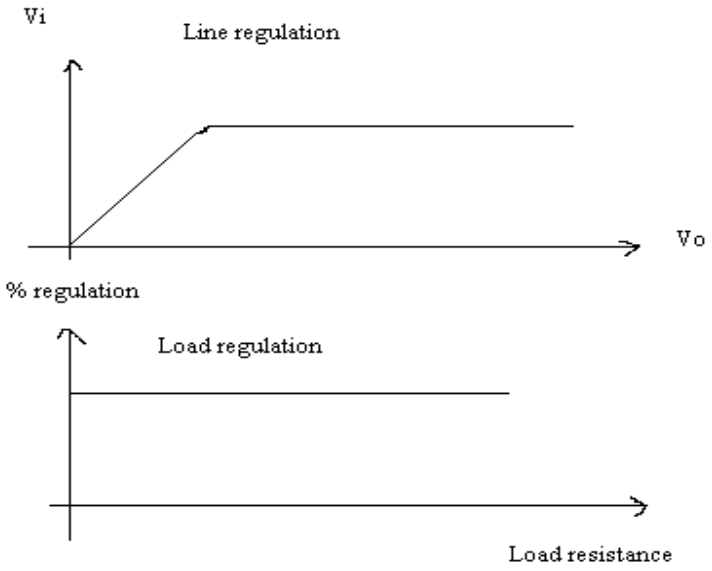
Line voltage (V)	Outputvoltage(V)

(2).LOAD REGULATION:

Regulated output(V)	Load current(mA)	Load resistance(KΩ)	Load regulation

% REGULATION=[(Vnl-Vfl)/Vfl]*100

MODEL GRAPH:



PRECAUTIONS:

1. While taking the readings of regulated output voltage load regulation ,keep the input voltage constant at15V.
2. Do not increase the input voltage more than 30 V while taking the reading for no load condition?

RESULT: Performed line and load regulation on 723 voltage regulator.

VIVA-VOICE QUESTIONS:

1. Define line regulation?
2. Define load regulation?
3. What are the applications of voltage regulators?

EXPERIMENT.13

13.Three Terminal Voltage Regulators (7805, 7809 And 7912)

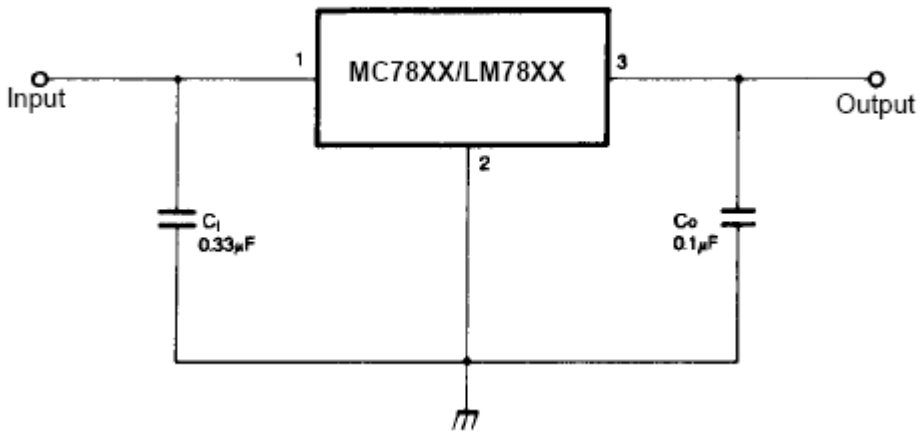
AIM:

To verify the operation of three terminal fixed voltage regulators 7805, 7809, 7912 and also to find out their line and load regulation.

APPARATUS:

S.No.	Name of the component	Range	Quantity
1.	7805	--	1
2.	7809	--	1
3.	7912	--	1
4.	Capacitors	0.33µf 0.1µf	1 1
5.	Multimeter	(0-30)v	1
6.	Power Supply		1

CIRCUIT DIAGRAM:



THEORY:

Three terminal voltage regulators have three terminals which are unregulated input (V_{in}), regulated output (V_o) and common or a ground terminal. These regulators do not require any feedback connections.

Positive voltage regulators:

78xx is the series of three terminal positive voltage regulators in which xx indicate the output voltage rating of the IC.

7805:

This is a three terminal regulator which gives a regulated output of +5V fixed. The maximum unregulated input voltage which can be applied to 7805 is 35V.

7809:

This is also three terminal fixed regulator which gives regulated voltage of +9V.

Negative voltage regulators:

79xx is the series of negative voltage regulators which gives a fixed negative voltage as output according to the value of xx.

7912:

This is a negative three terminal voltage regulator which gives a output of -12V.

Line Regulation:

It is defined as the change in the output voltage for a given change in the input voltage. It is expressed as a percentage of output voltage or in millivolts.

$\%R_L = \Delta V_o/\Delta V_{in}$ x 100

Load Regulation:

It is the change in output voltage over a given range of load currents that is from full load to no load. It is usually expressed in millivolts or as a percentage of output voltage.

$$\%R_{Load} = [(V_{nl}-V_{fl})/V_{nl}] \times 100$$

PROCEDURE:

1. Connect the circuit as shown in the figure.
2. Apply unregulated voltage from 7.5V to 35V and observe the output voltage.
3. Calculate the line and load regulation for the regulator.
4. Plot the graphs from the observations.
5. Repeat the same for the remaining regulators.

RESULTS: Hence performed various regulation operations ICs 7805, 7809, 7912.

VIVA-VOICE QUESTIONS:

1. What are three terminal voltage regulators?
2. Give applications of three terminal regulators.

KG REDDY College of Engineering & Technology

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Chilkur (Village), Moinabad (Mandal), R. R Dist., TS-501504

Accredited by NAAC

Academic Year: 2019-20
Section-A

Department of Electronics and Communication Engineering
II B. Tech Semesters: II Internal Exams

Day to Day lab evaluation

Name of the Lab: ICA
Roll No.: 18QM1A0402

Name of the Student: AADIMULAM SAINATH

S.No.	Name of the Experiment	Date of Experiment	Record of previous experiment (5 marks)	Execution of experiment (5 marks)	Viva-Voce (5 marks)	Total (15 marks)	Remarks by Faculty
1	Inverting and Non-Inverting Amplifiers using Op Amps	08-01-2020 5-02-2020	5	5	4	14	good
2	Adder and Subtractor using Op Amp.	22-01-2020	5	4	4	13	Results not shown
3	Comparators using Op Amp.	04-3-2020	5	4	5	14	good
4	Integrator Circuit using IC 741	29-01-2020	5	4	5	14	good
5	Differentiator Circuit using Op Amp.	29-01-2020	5	5	5	15	excellent
6	Active filter Applications-LPF, HPF (First Order)	22-01-2020	5	4	5	14	good
7	IC 741 waveform Generators-Sine, Square wave and Triangular Waves	29-01-2020	5	5	5	15	excellent
8	Mono-Stable Multivibrator using IC 555.	04-3-2020	5	4	4	13	good
9	Astable multivibrator using IC 555.	04-3-2020	5	4	5	14	good
10	Schmitt Trigger Circuits using IC 741.	11-3-2020	5	4	5	14	good
11	Voltage Regulator using IC 723	11-3-2020	5	4	5	14	good
12	Three terminal voltage regulators-7805, 7809, 7912	19-02-2020	5	4	5	14	good
	Average					14	

Faculty Member

HOD

DEPT. OF ELECTRONICS & COMMUNICATIONS ENGINEERING
K.G. REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
CHILKUR (V), MOINABAD, R.R. DIST. TS 501 504

Department of Electronics and Communication Engineering

Academic Year: 2019-20 II B. Tech Semesters: II Internal Section-A

Day to Day lab evaluation

Name of the Lab: ICA

Roll No.: 18QM1A0405 **Name of the Student: ALURI SINDHURA**

S.No.	Name of the Experiment	Date of Experiment	Record of previous experiment (5 marks)	Execution of experiment (5 marks)	Viva-Voce (5 marks)	Total (15 marks)	Remarks by Faculty
1	Inverting and Non-Inverting Amplifiers using Op Amps	08-01-2020	5	4	4	13	good
2	Adder and Subtractor using Op Amp.	22-01-2020	5	4	4	13	good
3	Comparators using Op Amp.	22-01-2020	5	4	4	13	good
4	Integrator Circuit using IC 741	22-01-2020	4	4	4	12	good
5	Differentiator Circuit using Op Amp.	5-02-2020	5	4	4	13	good
6	Active filter Applications-LPF, HPF (First Order)	5-02-2020	4	4	4	12	good
7	IC 741 waveform Generators-Sine, Square wave and Triangular Waves	5-02-2020	5	4	4	13	good
8	Mono-Stable Multivibrator using IC 555.	11-3-2020	5	4	4	13	good
9	Astable multivibrator using IC 555.	11-3-2020	4	4	4	12	good
10	Schmitt Trigger Circuits using IC 741.	11-3-2020	5	4	4	13	good
11	Voltage Regulator using IC 723		5	4	4	13	good
12	Three terminal voltage regulators-7805, 7809, 7912	19-02-2020	5	4	4	13	good
	Average					13	

Faculty Member **HOD**

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K.G. REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
CHILKUR (V), MOINABAD, R.R. DIST.-501 504.

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Chilkur (Village), Moinabad (Mandal), R. R. Dist. TS-501504

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Academic Year: 2019-20

Department of Electronics and Communication Engineering

II B. Tech Semesters: II Internal

Section-A

Day to Day lab evaluation

Name of the Lab: ICA

Roll No.: 18QM1A0406

Name of the Student: AMBATI BHARGAV

S.No.	Name of the Experiment	Date of Experiment	Record of previous experiment (5 marks)	Execution of experiment (5 marks)	Viva-Voce (5 marks)	Total (15 marks)	Remarks by Faculty
1	Inverting and Non-Inverting Amplifiers using Op Amps	08-01-2020	5	5	5	15	excellent
2	Adder and Subtractor using Op Amp.	29-01-2020	5	5	5	15	excellent
3	Comparators using Op Amp.	29-01-2020	5	4	5	14	good
4	Integrator Circuit using IC 741	22-01-2020	5	5	5	15	excellent
5	Differentiator Circuit using Op Amp.	22-01-2020	5	5	5	15	excellent
6	Active filter Applications-LPF, HPF (First Order)	29-01-2020	5	4	5	14	good
7	IC 741 waveform Generators-Sine, Square wave and Triangular Waves	04-3-2020	5	5	5	15	excellent
8	Mono-Stable Multivibrator using IC 555.	04-3-2020	5	5	5	15	excellent
9	Astable multivibrator using IC 555.	04-3-2020	5	5	5	15	excellent
10	Schmitt Trigger Circuits using IC 741.	11-3-2020	5	5	5	14	good
11	Voltage Regulator using IC 723	11-3-2020	5	5	5	15	excellent
12	Three terminal voltage regulators-7805, 7809, 7912	11-3-2020	5	5	5	15	excellent
	Average					15	

Faculty Member

HEAD
DEPT. OF ELECTRONICS & COMMUNICATION ENGINEERING
K.G. REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
CHILKUR (V), MOINABAD, R.R. DIST.-501 504

HOD

KG REDDY College of Engineering & Technology

DEPARTMENT

OF

ELECTRONICS AND COMMUNICATION ENGINEERING

NAME OF THE LABORATORY	**:**	**DIGITAL SYSTEM DESIGN LAB**
YEAR AND SEM	**:**	**II B.TECH I SEM**
REGULATION/LAB CODE	**:**	**R18/ EC307PC**

DIGITAL SYSTEM DESIGN LABORATORY MANUAL

HOD **PRINCIPAL**

KG REDDY College of Engineering & Technology

DEPARTMENT VISION

To be recognized as a full-fledged center for learning and research in various fields of Electronics and Communication Engineering through industrial collaboration and to provide consultancy for solving the real time socio-economic problems.

DEPARTMENT MISSION

- To provide innovative teaching and learning in the contemporary technologies in Electronics and Communication Engineering to support the professional aspirations of the students.
- To promote innovation through research and development among faculty and students by providing opportunities for inter-disciplinary learning in collaboration with industry.
- To encourage professional development of students that will inculcate ethical values and leadership skills while working with the community to address societal issues.

KG REDDY College of Engineering & Technology

Program Outcomes(PO's):

A graduate of the Electronics and Communication Engineering Program will demonstrate:

PO1: **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2: **Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6: **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: **Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one"s own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: **Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Educational Objectives (PEO's):

- **PEO 1:** To be equipped with skills for solving complex real-world problems related to VLSI, Embedded Systems, Signal/Image processing, and Digital and Wireless Communication.
- **PEO 2:** To develop professional skills that will equip them to succeed in their careers and encourage lifelong learning in advanced areas of Electronics and communications and related fields.
- **PEO 3:** To communicate effectively, work collaboratively and exhibit high levels of professionalism, moral and ethical responsibility.
- **PEO 4:** To develop the ability to understand and analyze engineering issues in a broader perspective with ethical responsibility towards sustainable development.

Program Specific Outcomes(PSO's)

- **PSO 1: Problem Solving Skills –** Graduates will be able to apply their knowledge in emerging electronics and communication engineering techniques to design solutions and solve complex engineering problems.
- **PSO 2: Professional Skills –** Graduate will be able to think critically, communicate effectively, and collaborate in teams through participation in co and extra-curricular activities.
- **PSO 3: Successful Career –** Graduates will possess a solid foundation in Electronics and Communications engineering that will enable them to grow in their profession and pursue lifelong learning through post-graduation and professional development.
- **PSO 4: Society Impact –** Graduate will be able to work with the community and collaborate to develop technological solutions that would promote sustainable development in the society.

EC307PC: DIGITAL SYSTEM DESIGN LAB

B. Tech. II Year I SEM **L T P C 0 0 2 1**

Note: Implement using digital ICs, all experiments to be carried out.

List of Experiments –

1. Realization of Boolean Expressions using Gates
2. Design and realization logic gates using universal gates
3. Generation of clock using NAND / NOR gates
4. Design a 4 – bit Adder/Subtractor
5. Design and realization of a 4 – bit gray to Binary and Binary to Gray Converter
6. Design and realization of an 8 bit parallel load and serial out shift register using flip-flops.
7. Design and realization of a Synchronous and Asynchronous counter using flip-flops
8. Design and realization of Asynchronous counters using flip-flops
9. Design and realization of 8x1 MUX using 2x1 MUX
10. Design and realization of 4 bit comparator
11. Design and Realization of a sequence detector-a finite state machine

Major Equipment's required for Laboratories:

1. 5 V Fixed Regulated Power Supply/ 0-5V or more Regulated Power Supply.
2. 20 MHz Oscilloscope with Dual Channel.
3. Bread board and components/ Trainer Kit.
4. Multimeter.

Course Outcomes (CO's)

Upon completion of this course, the student will be able to:

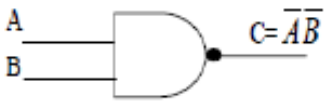
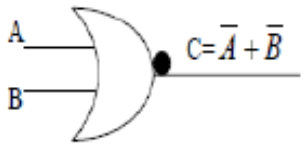
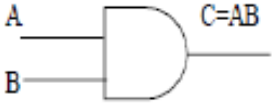
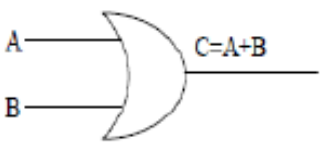
CO1: Derive Boolean Expression using Logic gates
CO2: Design Adder/Subtractor, Comparator and Multiplexer
CO3: Design shift registers, and counters using shift registers

Instruction to Digital System Design Laboratory

The basic logic gates are the building blocks of more complex logic circuits. These logic gates perform the basic Boolean functions, such as AND, OR, NAND, NOR, Inversion, Exclusive-OR, Exclusive-NOR. Fig. below shows the circuit symbol, Boolean function, and truth. It is seen from the Fig that each gate has one or two binary inputs, A and B, and one binary output, C. The small circle on the output of the circuit symbols designates the logic complement. The AND, OR, NAND, and NOR gates can be extended to have more than two inputs. A gate can be extended to have multiple inputs if the binary operation it represents is commutative and associative.

These basic logic gates are implemented as small-scale integrated circuits (SSICs) or as part of more complex medium scale (MSI) or very large-scale (VLSI) integrated circuits. Digital IC gates are classified not only by their logic operation, but also the specific logic- circuit family to which they belong. Each logic family has its own basic electronic circuit upon which more complex digital circuits and functions are developed. The following logic families are the most frequently used.

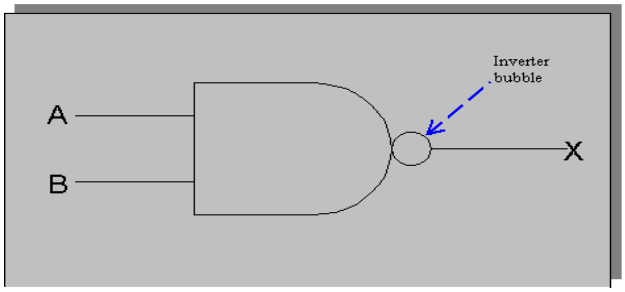
- TTL Transistor-transistor logic
- ECL Emitter-coupled logic
- MOS Metal-oxide semiconductor
- CMOS Complementary metal-oxide semiconductor

S.NO	GATE	SYMBOL	INPUTS		OUTPUT
			A	B	C
1.	NAND IC 7400		0	0	1
			0	1	1
			1	0	1
			1	1	0
2.	NOR IC 7402		0	0	1
			0	1	0
			1	0	0
			1	1	0
3.	AND IC 7408		0	0	0
			0	1	0
			1	0	0
			1	1	1
4.	OR IC 7432		0	0	0
			0	1	1
			1	0	1
			1	1	1

The NAND Gate:

The NAND, which is composed of two or more inputs and a single output, is a very popular logic element because it may be used as a universal function. That is, it may be employed to construct an inverter, an AND gate, an OR gate, or any combination of these functions. The term NAND is formed by the concatenation NOT-AND and implies an AND function with an inverted output. The standard symbol for the NAND gate is shown in Figure 1-7 and its truth table listed in Table 1-4. The logical operation of the NAND gate is such that the output is LOW (0) only when all the inputs are HIGH (1).

Standard logic symbol for NAND gate

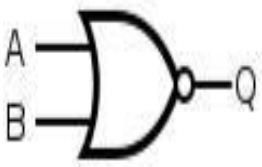


INPUT		OUTPUT
A	B	$X = \overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

Fig: Truth Table for NAND gate.

NOR GATE

A NOR gate is logically an inverted OR gate. By itself has the following truth table:



Truth Table

Input A	Input B	Output Q
0	0	1
0	1	0
1	0	0
1	1	0

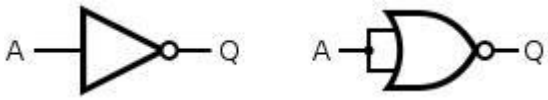
Making other gates by using NOR gates

A NOR gate is a universal gate, meaning that any other gate can be represented as a combination of NOR gates.

NOT

This is made by joining the inputs of a NOR gate. As a NOR is equivalent to an OR gate leading to NOT gate, this automatically sees to the "OR" part of the NOR gate, eliminating it from consideration and leaving only the NOT part.

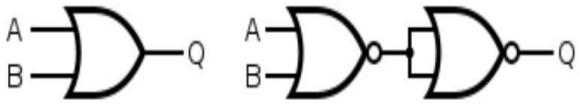
Desired Gate **NOR Construction**



OR

The OR gate is simply a NOR gate followed by a NOT gate.

Desired Gate **NOR Construction**

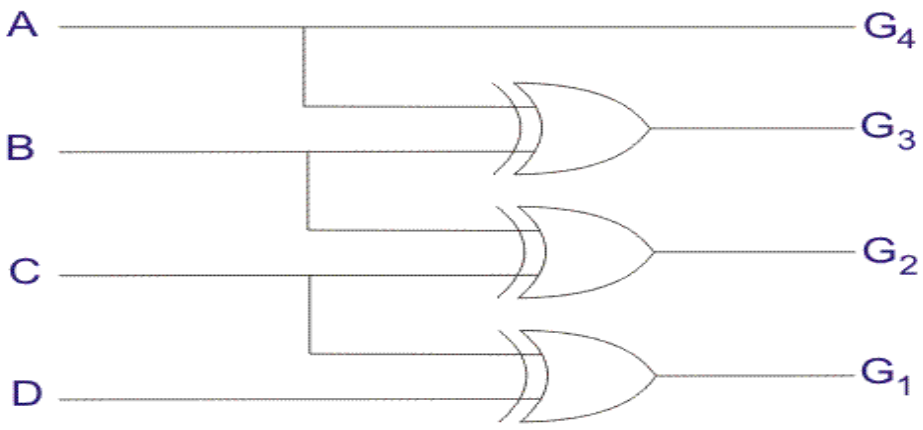


Truth Table

Input A	Input B	Output Q
0	0	0
0	1	1
1	0	1
1	1	1

Gray code converter: The logical circuit which converts binary code to equivalent Gray code is known as **binary to Gray code converter.** The Gray code is a non-weighted code. The successive Gray code differs in one bit position only that means it is a unit distance code. It is also referred as cyclic code. It is not suitable for arithmetic operations. It is the most popular of the unit distance codes. It is also a reflective code. An n-bit Gray Code can be obtained by reflecting an n-1 bit code about an axis after 2^{n-1} rows, and putting the MSB of 0 above the axis and the MSB of 1 below the axis. In **Gray to binary code converter**, input is multiplies Gray code and output is its equivalent binary code. Let us consider a 4 bit Gray to binary code converter. To design a 4 bit Gray to binary code converter, we first have to draw a conversion table.

Circuit diagram:



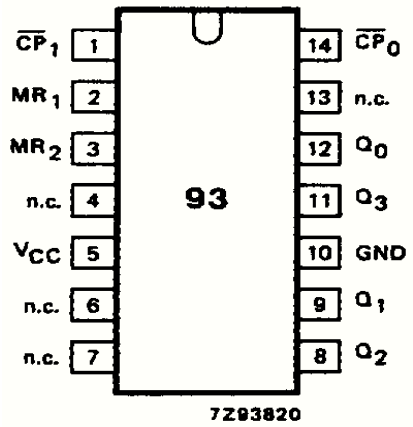
Logic Circuit for Binary to Gray Code Converter

Register: A register is simply a group of flip flops that can be used to store a binary number. A shift register is a group of flip flops connected such that the binary number can be entered (shifted) into the register and possibly shifted out. There are two ways to shift the data (bits in the binary number) from one place to another. The first method involves shifting the data 1bit at a time in a serial fashion, beginning with either MSB or LSB. This technique is referred to as serial shifting. The second method involves shifting all the data bits simultaneously and is referred to as parallel shifting. There are two ways to shift data into a register (serial or parallel) and similarly two ways to shift data out of the register. This leads to the construction of four basic types of registers.

1. Serial in – Serial out shift register.
2. Serial in – Parallel out shift register.
3. Parallel in – Serial out shift register.
4. Parallel in – Parallel out shift register.

Counter: A counter is a register capable of counting number of clock pulse arriving at its clock input. Counter represents the number of clock pulses arrived. An up/down counter is one that is capable of progressing in increasing order or decreasing order through a certain sequence. An up/down counter is also called bidirectional counter. Usually up/down operation of the counter is controlled by up/down signal. When this signal is high counter goes through up sequence and when up/down signal is low counter follows reverse sequence.
A 4-Bit Asynchronous Counter Count from 0 to 15 to Implement Binary Counter We Require 7493 IC. Pin Diagram Of These IC Is As Below.

Pin configuration of 74hct93:

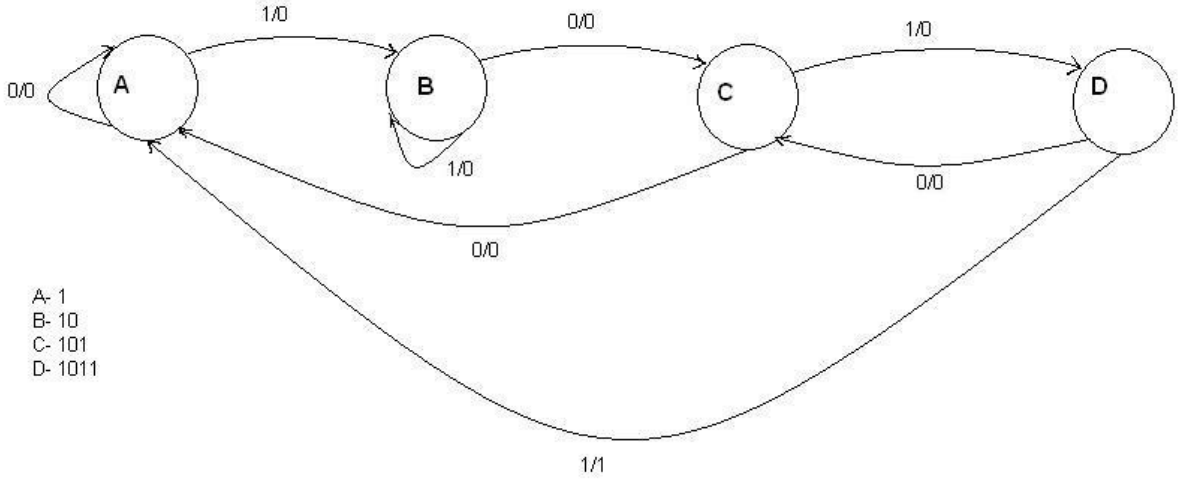


State Machine: A finite state machine is a digital system that can be characterized by a finite number of states, with transitions between states controlled by the present state and current input values. The output of the FSM will be a function of the current inputs and present state. In this lab you will design a finite state machine whose output will only be based on the present state. A sequence of data (one bit) will be the input into the machine. If the sequence "1101" occurs, the

output will be a 1. Otherwise the output will be a 0. Sequences can overlap –the 1 indicating the last bit of 1101 can also be the first bit of a trailing sequence. The FSM will be designed using the standard process of designing synchronous sequential digital systems. The finite state machine should be designed as follows: Registers are a storage device for data. Registers are used to hold the values of the states of the machine.

The canonical model for a synchronous sequential system is shown below. The present input, w, is fed into a combinational network, C1, which is the input into a series of FFs. The FFs are fed back through the combinational network as inputs, along with the input, w, as inputs to determine the next state of the registers. The system has two sets of outputs, the states and the output, z.

State machine for detecting the (non-overlapping)sequence "1011".



CONTENTS

EXPERIMENT1:
Realization of Boolean Expressions Using Gates

Aim: To realize the truth table of logic gates

Apparatus:

1. Logic gate kit
2. Patch cords

Theory:

A priority encoder is a circuit or algorithm that compresses multiple binary inputs into a smaller Logic gates are the basic building blocks of digital electronic circuits. A logic gate is a piece of an electronic circuit that can be used to implement Boolean expressions.

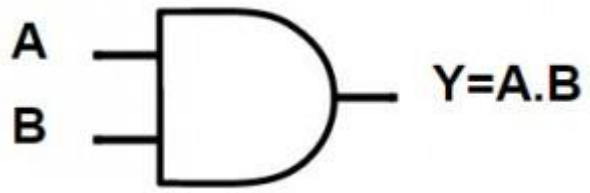
Laws and theorems of Boolean logic are used to manipulate the Boolean expressions and logic gates are used to implement these Boolean expressions in digital electronics. AND gate, OR gate and NOT gate are the three basic logic gates used in digital electronics.

Circuit diagram:

AND Gate

Logic AND gate is a basic logic gate of which the output is equal to the product of its inputs. This gate multiplies both of its inputs so this gate is used to find the multiplication of inputs in binary algebra.

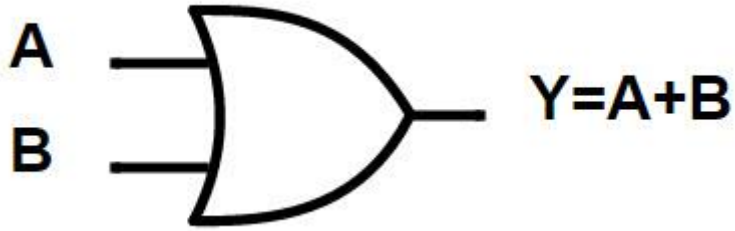
The output of an AND gate is HIGH only if both the inputs of the gate are HIGH. The output for all the other cases of the inputs is LOW. The logic symbol and the truth table of an AND gate is shown below.



A	B	Y=A.B
0	0	0
0	1	0
1	0	0
1	1	1

OR Gate

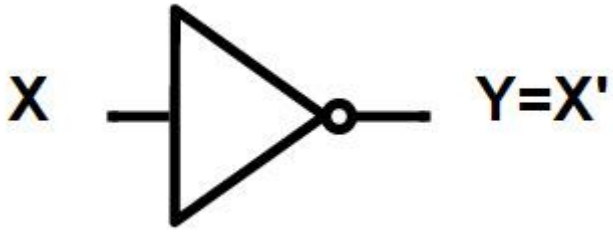
The output of the logic OR gate is equal to the sum of its inputs. This gate adds both of its inputs so this gate is used to find the summation or the addition of inputs in binary algebra. The output of an OR gate is HIGH if either of the inputs are HIGH. The output is LOW only when all the inputs are LOW. The logic symbol and the truth table of an OR gate is shown below.



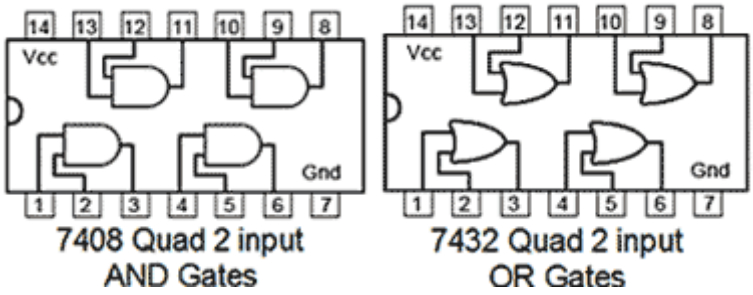
A	B	Y=A+B
0	0	0
0	1	1
1	0	1
1	1	1

NOT Gate

Logic NOT gate is a basic logic gate of which the output is equal to the inverse of its input. This gate produces the complement of the input. So this gate is used to represent the complement of variables in binary algebra. If the input is HIGH, the output is LOW and if the input is LOW, the output is HIGH. The logic symbol and the truth table of a NOT gate is shown below.



Pin diagram:



Procedure:

1. Make Connections as per the above Circuit Diagram
2. 0 to 15 Inputs are Connected to Inputs Switches
3. Connect EI (Pin no. 5) of 1st Encoder to E0 (Pin no.15) of 2nd Encoder
4. Connect A0, A1, A2 (Pin no's 9, 7, 6) of 1st Encoder to Inputs of Three AND (74LS08) Gate.
5. Connect A0, A1, A2 (Pin no's 9, 7, 6) of 2nd Encoder to Inputs of Three AND (74LS08) Gate.
6. Connect GS (Pin no.14) of Both Encoders to the Input of Fourth AND (74LS08) Gate.
7. Connect Outputs of Three AND (74LS08) Gates to Connect Output Switches
8. Connect GS (Pin no.14) of 2nd Encoder to Output Switch
9. Give Inputs as per the Truth Table & Observe Output.

Result: Hence verified the truth table of Priority Encoder.

Viva Questions:

1. What is logic gate?

2. What are universal gates?

3. Design AND, OR, NOT gate using universal logic gates?

4. How many inputs and Outputs in AND gate?

EXPERIMENT2:

Design and Realization Logic Gates Using Universal Gates

Aim: To verify the truth table of logic gate using NOR/NAND gate.

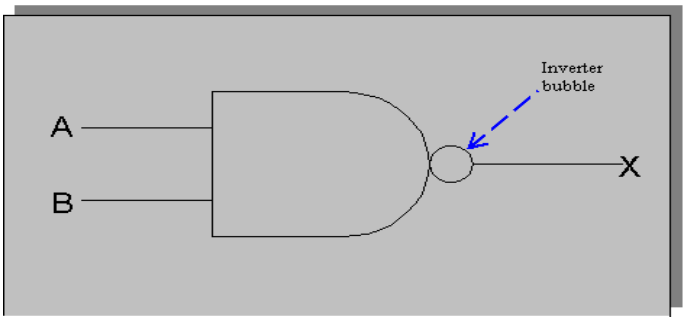
Apparatus:

1. Logic gate kit
2. Patch Cords

Theory:

The NAND Gate:

The NAND, which is composed of two or more inputs and a single output, is a very popular logic element because it may be used as a universal function. That is, it may be employed to construct an inverter, an AND gate, an OR gate, or any combination of these functions. The term NAND is formed by the concatenation NOT-AND and implies an AND function with an inverted output. The standard symbol for the NAND gate is shown in Figure 1-7 and its truth table listed in Table 1-4. The logical operation of the NAND gate is such that the output is LOW (0) only when all the inputs are HIGH (1).

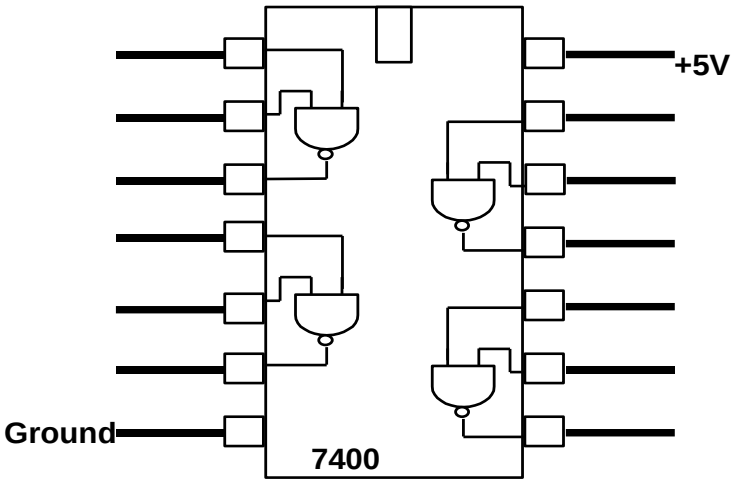


Standard logic symbol for NAND gate

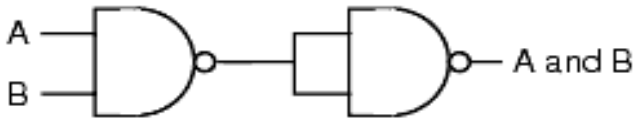
INPUT		OUTPUT
A	B	$X = \overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

Fig: Truth Table for NAND gate.

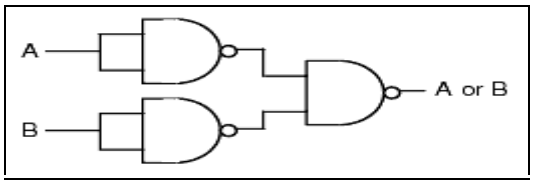
Pin diagram for 7400 Quad NAND gate IC:-



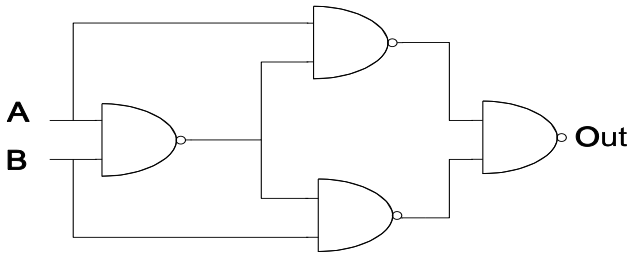
1. **Implementing AND gate using NAND gate:**



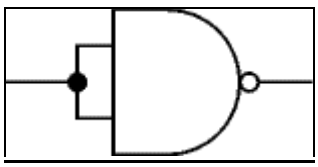
2. **Implementing OR gate using NAND gate:**



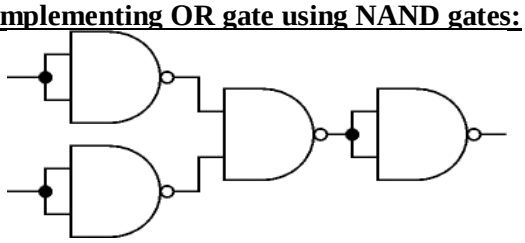
3. **Implementing X- OR gate using NAND gate:**



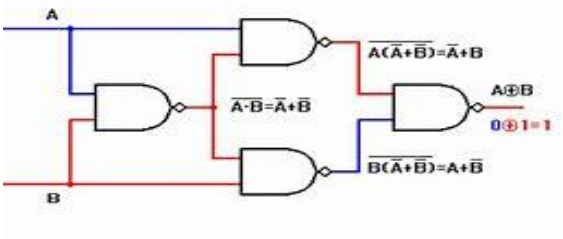
4. **Implementing NOT gate using NAND gate:**



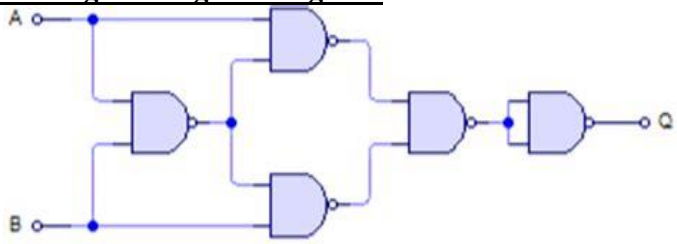
5. **Implementing OR gate using NAND gates:**



6. **Implementing XOR gate using NAND gates:**



7. **Implementing XNOR gate using NAND gates:**

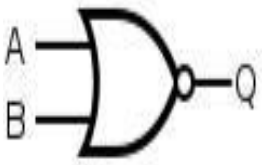


Procedure:-

1. Place the IC on IC Trainer Kit.
2. Connect V_{CC} and ground to respective pins of IC Trainer Kit.
3. Connect the inputs to the input switches provided in the IC Trainer Kit.
4. Connect the outputs to the switches of O/P LEDs,
5. Apply various combinations of inputs according to the truth table and observe condition of LEDs.
6. Disconnect output from the LEDs and note down the corresponding multimeter voltage readings for various combinations of inputs.

NOR GATE

A NOR gate is logically an inverted OR gate. By itself has the following truth table:



Truth Table

Input A	Input B	Output Q
0	0	1
0	1	0
1	0	0

1 1 0

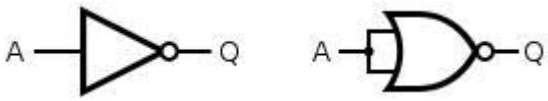
Making other gates by using NOR gates

A NOR gate is a universal gate, meaning that any other gate can be represented as a combination of NOR gates.

NOT

This is made by joining the inputs of a NOR gate. As a NOR is equivalent to an OR gate leading to NOT gate, this automatically sees to the "OR" part of the NOR gate, eliminating it from consideration and leaving only the NOT part.

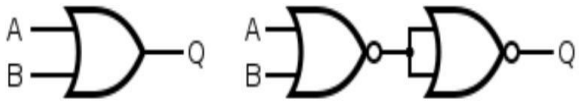
Desired Gate **NOR Construction**



OR

The OR gate is simply a NOR gate followed by a NOT gate.

Desired Gate **NOR Construction**

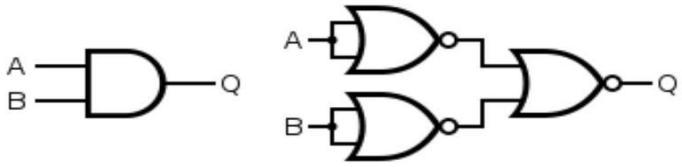


Truth Table

Input A	Input B	Output Q
0	0	0
0	1	1
1	0	1
1	1	1

AND An AND gate gives a 1 output when both inputs are 1; a NOR gate gives a 1 output only when both inputs are 0. Therefore, an AND gate is made by inverting the inputs to a NOR gate.

Desired Gate **NOR Construction**



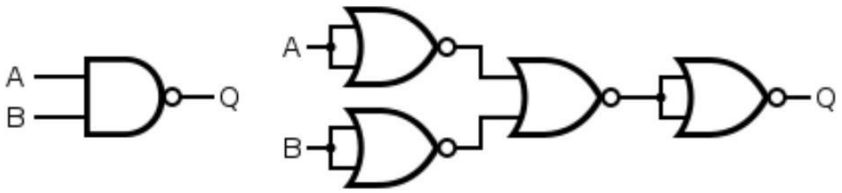
Truth Table

Input A	Input B	Output Q
0	0	0
0	1	0
1	0	0

1 1 1

NAND A NAND gate is made using an AND gate in series with a NOT gate:

Desired Gate **NOR Construction**



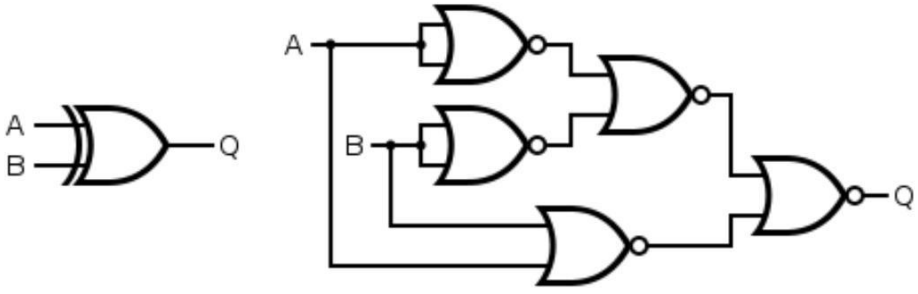
Truth Table

Input A	Input B	Output Q
0	0	1
0	1	1
1	0	1
1	1	0

XOR

An XOR gate is made by connecting the output of 3 NOR gates (connected as an AND gate) and the output of a NOR gate to the respective inputs of a NOR gate. This expresses the logical formula (A AND B) NOR (A NOR B). This construction entails propagation delay three times that of a single NOR gate.

Desired Gate **NOR Construction**



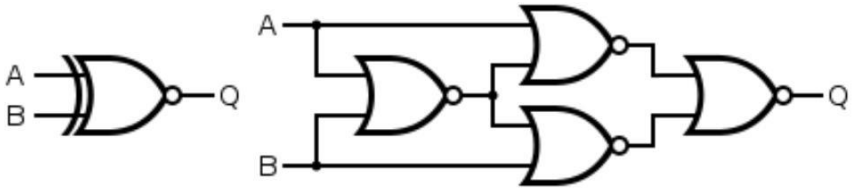
Truth Table

Input A	Input B	Output Q
0	0	0
0	1	1
1	0	1
1	1	0

XNOR

An XNOR gate can be constructed from four NOR gates implementing the expression "(A NOR N) NOR (B NOR N) where N = A NOR B". This construction has a propagation delay three times that of a single NOR gate, and uses more gates.

Desired Gate **NOR Construction**



Truth Table

Input Input Output

A	**B**	**Q**
0	0	1
0	1	0
1	0	0

Precautions: -

1. All the connection should be tight.
2. It should be care that the values of the components of the circuit is does not exceed to their ratings (maximum value).
3. Before the circuit connection it should be check out working condition of all the Component.

Result:- Designing of basic gates by using of NOR gate is successfully done .

Viva Questions:

1. What is logic gate?
2. What are universal gates?
3. Design AND, OR, NOT gate using universal logic gates?

EXPERIMENT3:

Generation of Clock Using NAND / NOR Gates

AIM: To verify the generation of clocks using gate.

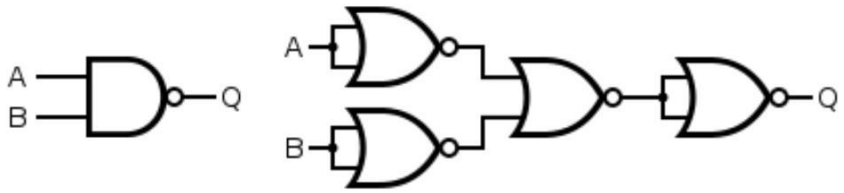
APPARATUS: Trainer kit and Patch cords

Theory:

	0	1 0
1	0	0
1	1	1

NAND A NAND gate is made using an AND gate in series with a NOT gate:

Desired Gate **NOR Construction**



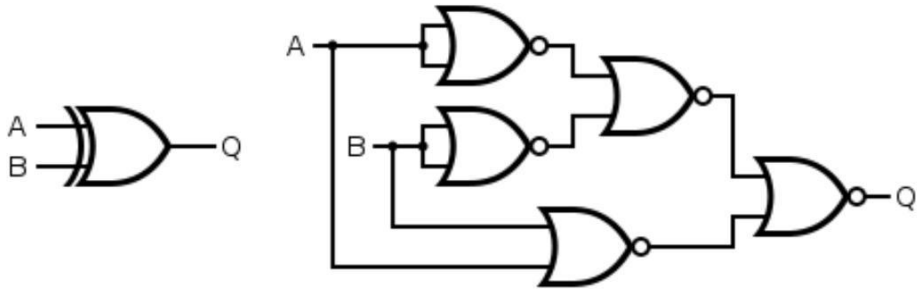
Truth Table

Input A	Input B	Output Q
0	0	1
0	1	1
1	0	1
1	1	0

XOR

An XOR gate is made by connecting the output of 3 NOR gates (connected as an AND gate) and the output of a NOR gate to the respective inputs of a NOR gate. This expresses the neither logical formula (A AND B) NOR (A NOR B). This construction entails propagation neither delay three times that of a single NOR gate.

Desired Gate **NOR Construction**



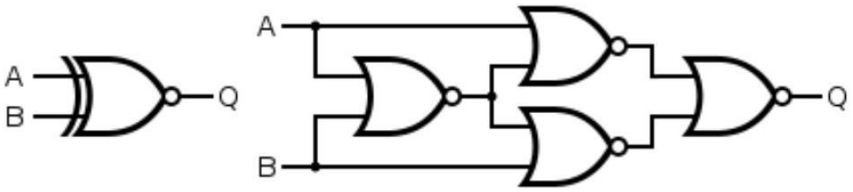
Truth Table

Input A	Input B	Output Q
0	0	0
0	1	1
1	0	1
1	1	0

XNOR

An XNOR gate can be constructed from four NOR gates implementing the expression "(A NOR N) NOR (B NOR N) where N = A NOR B". This construction has a propagation delay three times that of a single NOR gate, and uses more gates.

Desired Gate **NOR Construction**



Truth Table

Input A	Input B	Output Q
0	0	1
0	1	0
1	0	0

Precautions: -

1. All the connection should be tight.
2. It should be care that the values of the components of the circuit is does not exceed to their ratings (maximum value).
3. Before the circuit connection it should be check out working condition of the entire Component.

Result:- Designing of basic gates by using of NOR gate is successfully done .

Viva Questions:

1. What is logic gate?
2. What are universal gates?
3. Design AND, OR, NOT gate using universal logic gates?

EXPERIMENT4:
Design a 4 – Bit Adder / Subtractor

Aim: To verify the truth table of Adder and Subtractor.

Apparatus:

1. Adder / Subtractor kit
2. Patch cords.

Theory:

Having an n-bit adder for A and B, then $S = A + B$. Then, assume the numbers are in two's complement. Then to perform $B - A$, two's complement theory says to invert each bit with a NOT gate then add one. This yields $S = B + A + 1$, which is easy to do with a slightly modified adder.

By preceding each A input bit on the adder with a 2-to-1 multiplexer where:

- Input 0 (I_0) is A
- Input 1 (I_1) is A

That has control input D that is also connected to the initial carry, and then the modified adder performs

- addition when $D = 0$, or
- Subtraction when $D = 1$.

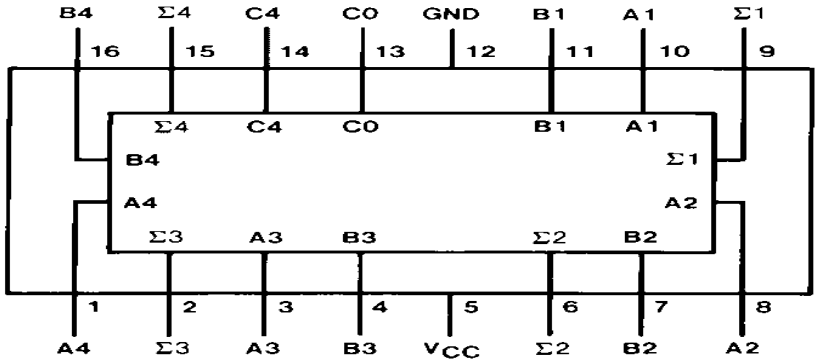
This works because when $D = 1$ the A input to the adder is really 'A' and the carry in is 1. Adding B to A and 1 yields the desired subtraction of $B - A$.

A way you can mark number A as positive or negative without using a multiplexer on each bit is to use an XOR gate to precede each bit instead.

- The first input to the XOR gate is the actual input bit
- The second input to the XOR gate for each is the control input D

This produces the same truth table for the bit arriving at the adder as the multiplexer solution does since the XOR gate output will be what the input bit is when $D = 0$ and the inverted input bit when $D = 1$.

Pin diagram:



Truth table:

INPUTS									OUTPUTS				
Cin	**A0**	**A1**	**A2**	**A3**	**B0**	**B1**	**B2**	**B3**	**S0**	**S1**	**S2**	**S3**	**OUT**
0	0	0	0	1	1	0	0	1	1	0	0	0	1
1	0	0	0	1	1	0	0	1	0	1	0	0	1

NOTE: You may add any two 4-bit binary numbers by making the cin to logic 0/1.

Procedure:

1. Connect the inputs A0, A1, A2, A3, B0, B1, B2, B3 and Cin to the input switches.(A0-A3 represents 1binary input and B0-B3 represents another binary input, Cin represents carry input)
2. Connect the Outputs S0, S1, S2, S3 and C4 (0ut on the board) to the output switches.
3. Feed the logic inputs and note down the outputs.

NOTE:

1. When the Cin is at logic 0, the output will be displaying the carry output but doesn't add with the binary inputs given.
2. When the Cin is at logic 1, the Output will be displayed by adding the carry.

Result: Hence performed the 4-bit Binary Addition using IC 7483.

Viva Questions:

1. What is adder?
2. Sum equation of 1-bit full adder
3. Carry equation of 1-bit full adder
4. General sum and carry equation

EXPERIMENT 5:

Design and Realization of a 4 – Bit Gray to Binary and Binary to Gray Converter

Aim: Observe Binary to Gray & Gray to Binary Code Conversion.

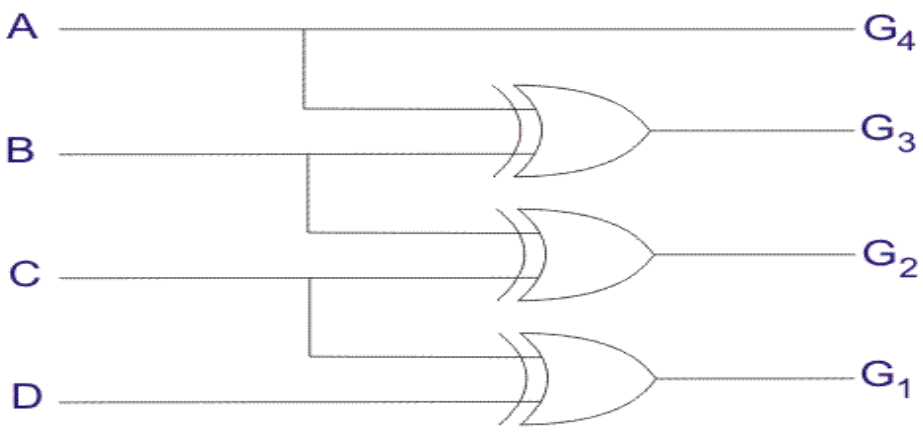
Apparatus:

1. GRAY-BINARY-GRAY Kit
2. Patch Cords

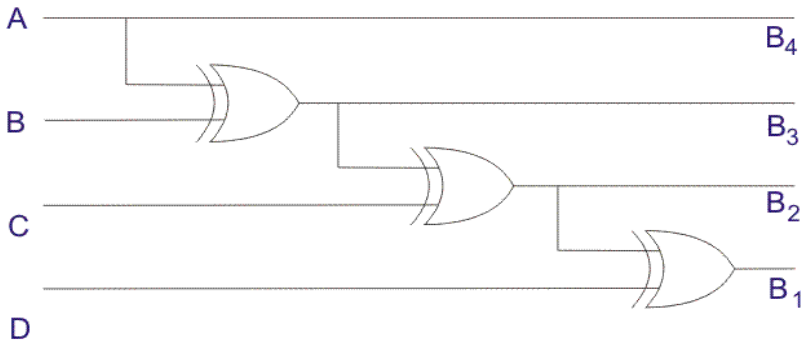
Theory:

The logical circuit which converts binary code to equivalent gray code is known as **binary to gray code converter.** The gray code is a non weighted code. The successive gray code differs in one bit position only that means it is a unit distance code. It is also referred as cyclic code. It is not suitable for arithmetic operations. It is the most popular of the unit distance codes. It is also a reflective code. An n-bit Gray Code can be obtained by reflecting an n-1 bit code about an axis after 2^{n-1} rows, and putting the MSB of 0 above the axis and the MSB of 1 below the axis. In **Gray to binary code converter**, input is a multiplies gray code and output is its equivalent binary code. Let us consider a 4 bit gray to binary code converter. To design a 4 bit gray to binary code converter, we first have to draw a conversion table.

Circuit diagram:



Logic Circuit for Binary to Gray Code Converter



Logic Circuit for Gray to Binary Code Converter

Truth table:

INPUTS				OUTPUTS			
BINARY CODE				GRAY CODE			
A	B	C	D	G1	G2	G3	G4
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

INPUTS				OUTPUTS			
GRAY CODE				BINARY CODE			
A	B	C	D	B4	B3	B2	B1
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1

Procedure:

Binary to Gray:

1. Connect Inputs (A,B,C,D) to Input Switches (Red LED)
2. Connect Outputs (G1,G2,G3,G4) to Output Switches (Green LED)
3. Give Binary Inputs at A, B, and C, D & Observe Gray Code Outputs as per Truth Table.

Gray to binary:

1. Connect Inputs (A,B,C,D) to Input Switches (Red LED)
2. Connect Outputs (B1,B2,B3,B4) to Output Switches (Green LED)
3. Give Gray Code Inputs at A, B, and C, D & Observe Binary Code Outputs as per Truth Table.
4.

Result: Binary to Gray & Gray to Binary Code Conversion is verified.

Viva Questions:

1. What is Binary?
2. Decimal code?
3. Explain binary to Decimal code converter
4. Explain Decimal to binary code converter

EXPERIMENT6:
Design and Realization of an 8 Bit Parallel Load and Serial out Shift Register Using Flip-Flops

Aim: To Verify the Truth Table of Shift Register.

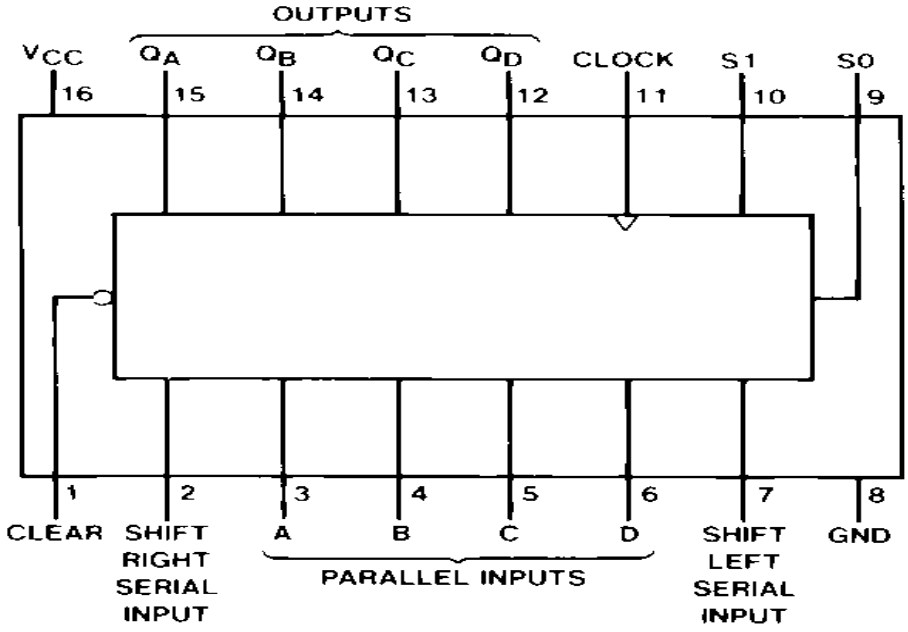
Apparatus:

1. Shift Register Trainer kit
2. Patch chords,
3. Clock Pulse Generator.

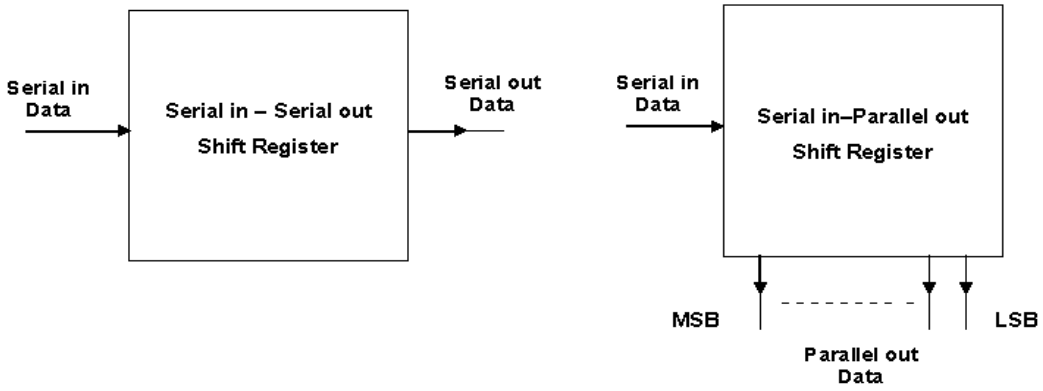
Theory:

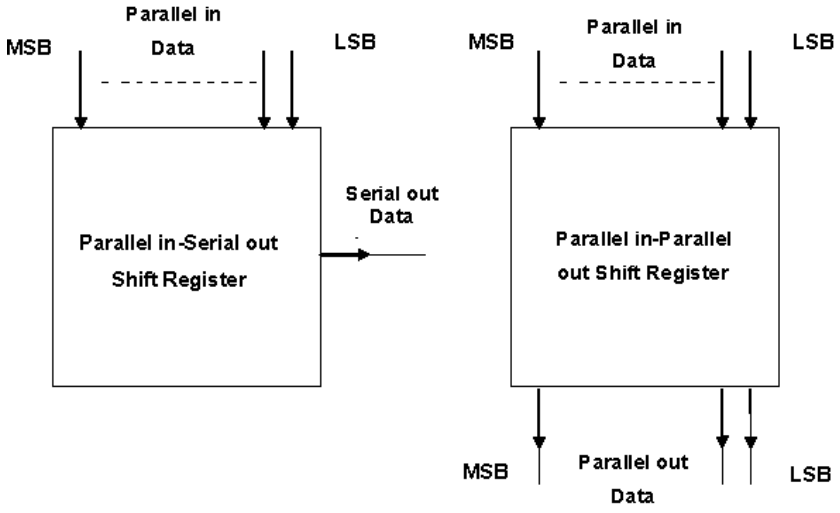
A register is simply a group of flip flops that can be used to store a binary number. A shift register is a group of flip flops connected such that the binary number can be entered (shifted) into the register and possibly shifted out. There are two ways to shift the data (bits in the binary number) from one place to another. The first method involves shifting the data 1bit at a time in a serial fashion, beginning with either MSB or LSB. This technique is referred to as serial shifting. The second method involves shifting all the data bits simultaneously and is referred to as parallel shifting. There are two ways to shift data into a register (serial or parallel) and similarly two ways to shift data out of the register. This leads to the construction of four basic types of registers.

1. Serial in – Serial out shift register.
2. Serial in – Parallel out shift register.
3. Parallel in – Serial out shift register.
4. Parallel in – Parallel out shift register.



Block diagram of 4 types of shift registers (n-bit).





Truth table:

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				QA	QB	QC	QD
	S1	S0		LEFT	RIGHT	A	B	C	D				
H	X	X	⌞	X	X	X	X	X	X	QA0	QB0	QC0	QD0
H	H	H		X	X	a	b	c	d	a	b	c	d

			⌐									
H	L	H	⌐	X	H	X	X	X	X	H	QAn	QBn	QCn
H	L	H	⌐	X	L	X	X	X	X	L	QAn	QBn	QCn
H	H	L	⌐	H	X	X	X	X	X	QBn	QCn	QDn	H
H	H	L	⌐	L	X	X	X	X	X	QBn	QCn	QDn	L
H	L	L	X	X	X	X	X	X	X	QA0	QB0	QC0	QD0

Procedure:

1. Derive the wiring diagram.
2. Connect Input terminals to the Logic Input Sockets.
   S1, S0, SERIAL LEFT, SERIAL RIGHT, PARALLEL DATA - A, B, C and D to Logic Input Sockets.
3. Connect CLEAR to VCC.
4. Connect External Clock to the CLOCK Terminal.
5. Connect QA, QB, QC and QD to the Logic Output terminals.
6. Observe output changes at O/P Terminals with given Truth Table.

Result: Verified the Truth Table of Universal Shift Register.

Viva Questions:

1. What is shift resister?

2. Explain PIPO, SIPO, SISO and SIPO

EXPERIMENT7:

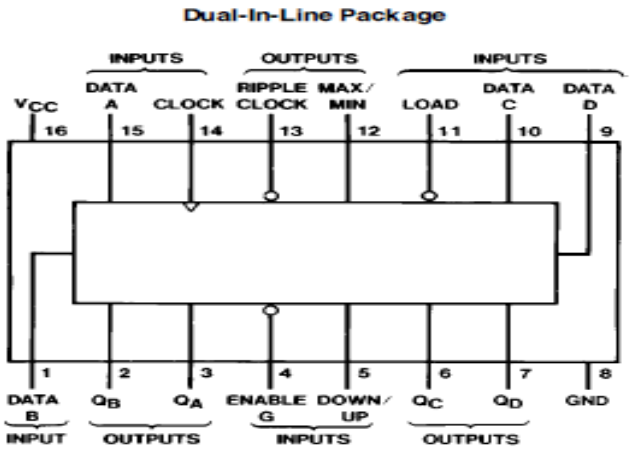
Design and Realization of a Synchronous and Asynchronous Counter Using Flip-Flops

Aim: To verify the truth table of 4-bit Synchronous Counter.

Apparatus: Counter kit and Patch Cords

Theory:
A counter is a register capable of counting number of clock pulse arriving at its clock input. Counter represents the number of clock pulses arrived. An up/down counter is one that is capable of progressing in increasing order or decreasing order through a certain sequence. An up/down counter is also called bidirectional counter. Usually up/down operation of the counter is controlled by up/down signal. When this signal is high counter goes through up sequence and when up/down signal is low counter follows reverse sequence.

Connection diagram:



Procedure:

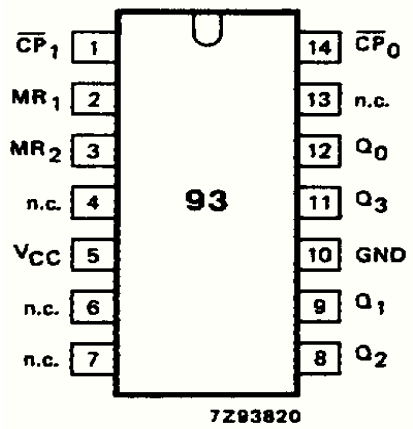
1. Connect the inputs A, B, C, D, G, max/min, load and up/down to the logic input switches and outputs Qa Qb, Qc and Qd to the output logic switches.
2. Keep load input high.
3. When up input (on the board) is fed with logic 0 then the count is “Up” count.
4. When up input (on the board) is fed with logic 1 then the count is “down” count.
5. This Count is achieved with Pulsar switch (instead of the clock, pulsar input has to be connected and the output changes with every pulse).

Function Table: (Up Count)

COUNT	OUTPUTS			
	Qd	Qc	Qb	Qa
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

COUNT	OUTPUTS			
	Qd	Qc	Qb	Qa
0	H	H	H	H
1	H	H	H	L
2	H	H	L	H
3	H	H	L	L
4	H	L	H	H
5	H	L	H	L
6	H	L	L	H
7	H	L	L	L
8	L	H	H	H
9	L	H	H	L
10	L	H	L	H
11	L	H	L	L
12	L	L	H	H
13	L	L	H	L
14	L	L	L	H
15	L	L	L	L

Pin configuration of 74hct93:



Truth table:

Reset I/P		**Outputs**			
MR1	**MR2**	**Q3**	**Q2**	**Q1**	**Q0**
H	H	L	L	L	L
L	H	COUNT			
H	L	COUNT			
L	L	COUNT			

Count table:

COUNT	**OUTPUTS**			
	Q3	**Q2**	**Q1**	**Q0**
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Result: Hence Verified The Truth Table Of 4 Bit Binary Asynchronous Counter.

Viva Questions:

1. What is Asynchronous counter?
2. Explain up counter
3. Explain down counter
4. Synchronous counter

EXPERIMENT8:

Design and Realization of Asynchronous Counter Using Flip-Flops

Aim: To Verify The Truth Table Of 4 Bit Asynchronous Counter.

.

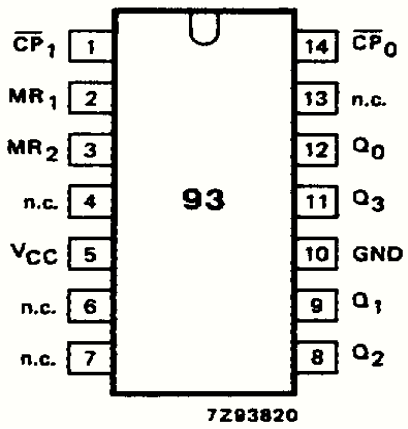
Apparatus: Counter (MTS) kit and patch cords

Theory:

A counter is a register capable of counting number of clock pulse arriving at its clock input. Counter represents the number of clock pulses arrived. An up/down counter is one that is capable of progressing in increasing order or decreasing order through a certain sequence. An up/down counter is also called bidirectional counter. Usually up/down operation of the counter is controlled by up/down signal. When this signal is high counter goes through up sequence and when up/down signal is low counter follows reverse sequence.

A 4-Bit Asynchronous Counter Count from 0 to 15 to Implement Binary Counter We Require 7493 IC. Pin Diagram Of These IC Is As Below.

Pin configuration of 74hct93:



Procedure:

1. Connect the Inputs MR1, MR2, To the Logic Input Switches and Outputs Qo, Q1, Q2, and Q3 to the Logic Outputs.
2. Feed the Logic Signals 0 Or 1 As Shown In The Truth Table.
3. Monitor the Outputs Q0, Q1, Q2, Q3.
4. Verify The Truth Table.

NOTE:

1. Connect $\overline{CP1}$ To Qo
2. Pulse Input Is Connected To Pin 14 ($\overline{CP0}$)
3. When The Count Output Is Present Count Can Be Observed

With Every Pulse (16 Pulses)

Truth table:

Reset I/P		Outputs			
MR1	**MR2**	**Q3**	**Q2**	**Q1**	**Q0**
H	H	L	L	L	L
L	H	COUNT			
H	L	COUNT			
L	L	COUNT			

Count table:

COUNT	**OUTPUTS**			
	Q3	**Q2**	**Q1**	**Q0**
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Result: Hence Verified The Truth Table Of 4 Bit Binary Asynchronous Counter.

Viva Questions:

1. What is Asynchronous counter
2. What are the four bit binary
3. Example of four bit binary

EXPERIMENT9:

Design and Realization Of 8x1 Mux Using 2x1 Mux

Aim: To verify the truth table of Multiplexer.

Apparatus: Multiplexer kit and Patch Cords.

Theory:

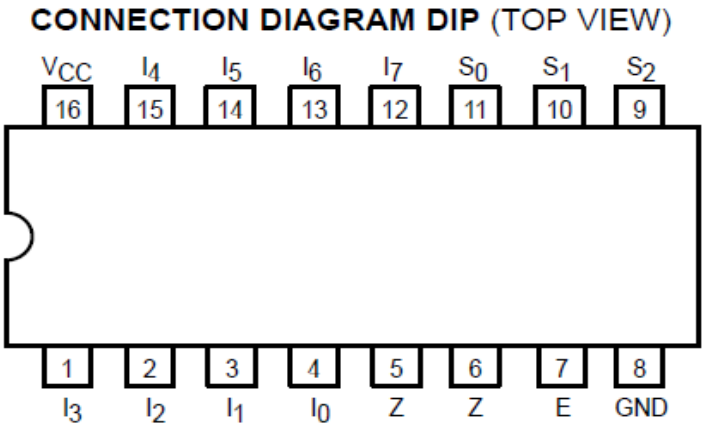
TTL/MSI SN54/74LS151 is a high speed 8-input Digital Multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. The LS151 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

- Schottky Process for High Speed
- Multifunction Capability
- On-Chip Select Logic Decoding
- Fully Buffered Complementary Outputs
- Input Clamp Diodes Limit High Speed Termination Effects

Functional Description

The LS151 is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S0, S1, and S2. Both assertion and negation outputs are provided. The Enable input (E) is active LOW. When it is not activated, the negation output is HIGH and the assertion output is LOW regardless of all other inputs.

Pin Diagram



$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Procedure:

1. Connect Inputs S2,S1,S0,I0, I1,I2,I,3 I4,I5,I6, I7 and Enable (E) to Logic Input Sockets.
2. Connect Output terminal Z & $\overline{Z}$ to Logic Output Sockets.
3. Verify output with given Truth Table.

Result: Hence verified the truth table of Multiplexer.

Viva Questions:

1. What is Mux?

2. Define Demux?

3. Design 4:1 mux using logic gates and write the equation

EXPERIMENT10:

Design and Realization of 4 Bit Comparator

Aim: To verify the truth table of 4-bit Comparator.

Apparatus:

1. Comparator kit
2. Patch Cords

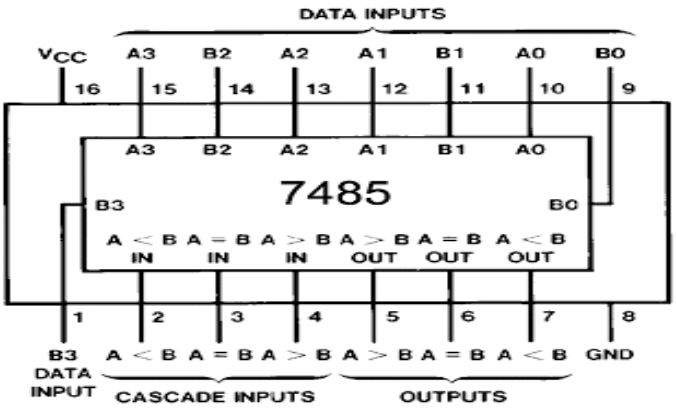
Theory:

The SN54/74LS85 is a 4-Bit Magnitude Camparator which compares two 4-bit words (A, B), each word having four Parallel Inputs ($A_0 - A_3$, $B_0 - B_3$); A_3, B_3 being the most significant inputs. Operation is not restricted to binary codes, the device will work with any monotonic code. Three Outputs are provided: "A greater than B" ($O_{A>B}$), "A less than B" ($O_{A<B}$), "A equal to B" ($O_{A=B}$). Three Expander Inputs, $I_{A>B}$, $I_{A<B}$, $I_{A=B}$, allow cascading without external gates. For proper compare operation, the Expander Inputs to the least significant position must be connected as follows: $I_{A<B} = I_{A>B} = L$, $I_{A=B} = H$. For serial (ripple) expansion, the $O_{A>B}$, $O_{A<B}$ and $O_{A=B}$ Outputs are connected respectively to the $I_{A>B}$, $I_{A<B}$, and $I_{A=B}$ Inputs of the next most significant comparator, as shown in Figure 1. Refer to Applications section of data sheet for high speed method of comparing large words.

The Truth Table on the following page describes the operation of the SN54/74LS85 under all possible logic conditions. The upper 11 lines describe the normal operation under all conditions that will occur in a single device or in a series expansion scheme. The lower five lines describe the operation under abnormal conditions on the cascading inputs. These conditions occur when the parallel expansion technique is used.

- Easily Expandable
- Binary or BCD Comparison
- $O_{A>B}$, $O_{A<B}$, and $O_{A=B}$ Outputs Available

Pin diagram :



Truth table:

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3,B3	**A2,B2**	**A1,B1**	**A0,B0**	**A>B**	**A<B**	**A=B**	**A>B**	**A<B**	**A=B**
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L

Procedure:

1. Connect Inputs (A0,A1,A2,A3,B0,B1,B2,B3) to Input Switches

2. Connect Cascade Inputs (A<B,A>B,A=B) to Input Switches
3. Connect Outputs (A<B,A>B,A=B) to Output Switches
4. Observe the Truth Table.

Result: Verified the truth table of Comparator.

Viva Questions:

1. What is comparator?

2. Design 2bit comparator using logic gates

3 Number of outputs for the comparator?

EXPERIMENT 11.

Design and Realization of a Sequence Detector-A Finite State Machine

Aim: To verify the finite states of sequence detector.

Apparatus: A DIGILAB BASYS board

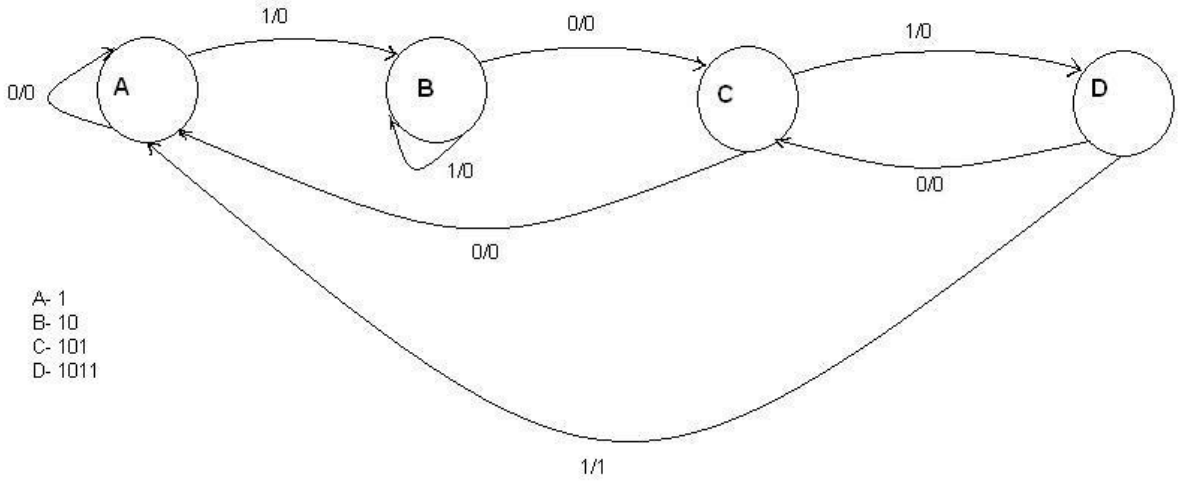
A PC running the Xilinx ISE CAD tools

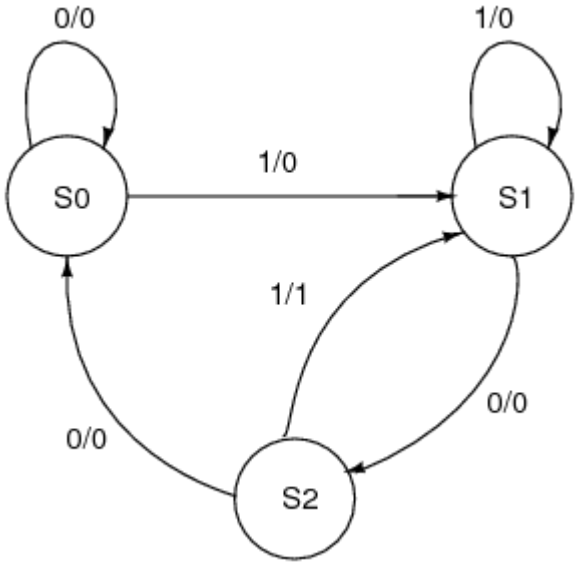
Theory:

A finite state machine is a digital system that can be characterized by a finite number of states, with transitions between states controlled by the present state and current input values. The output of the FSM will be a function of the current inputs and present state. In this lab you will design a finite state machine whose output will only be based on the present state. A sequence of data (one bit) will be the input into the machine. If the sequence "1101" occurs, the output will be a 1. Otherwise the output will be a 0. Sequences can overlap –the 1 indicating the last bit of 1101 can also be the first bit of a trailing sequence. The FSM will be designed using the standard process of designing synchronous sequential digital systems. The finite state machine should be designed as follows: Registers are a storage device for data. Registers are used to hold the values of the states of the machine.

The canonical model for a synchronous sequential system is shown below. The present input, w, is fed into a combinational network, C1, which is the input into a series of FFs. The FFs are fed back through the combinational network as inputs, along with the input, w, as inputs to determine the next state of the registers. The system has two sets of outputs, the states and the output, z.

State machine for detecting the (non-overlapping)sequence "1011".





Two different types of synchronous sequential machines exist. Moore machines have outputs that are only dependent on the present state (the blue line is not necessary for this type of system). Alternatively, systems can be designed with the outputs dependent on the present state as well as the present input, Mealy machines. Here the blue line would be used.
In this week's lab, we are designing the Moore type of FSM. Mealy machines typically allow for fewer states than Moore machines.
We want to design a sequence detector that will output a 1 if the sequence "1101" is detected in the data coming in. In the system shown above, a 1 would be output during the next clock cycle.

Result: Verified the finite states of sequence detector.

Viva Questions:

1. What is FSM?

2. Define MOD N?

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Department of Electronics and Communication Engineering

Academic Year: 2019-20 | II B. Tech | Semester: II | Internal -I | Section-A

Day to Day Lab Evaluation

Name of the Lab: DSD LAB
Roll No.: 18QM1A0402 **Name of the Student:** AadimulamSainath

S. No.	Name of the Experiment	Date of Experiment	Record of previous experiment (5 marks)	Execution of experiment (5 marks)	Viva-voce (5 marks)	Total (15 marks)	Remarks by Faculty
1	Realization of Boolean Expressions using Gates	23-8-2019	5	5	4	14	Not good enough in viva-voce
2	Design and realization logic gates using universal gates	23-8-2019	4	5	5	14	Late submission
3	Generation of clock using NAND / NOR gates	6-9-2019	5	5	5	15	Good in laboratory work
4	Design a 4 – bit Adder / Subtractor	6-9-2019	3	5	5	13	Late submission
5	Design and realization of a 4 – bit gray to Binary and Binary to Gray Converter	23-8-2019	5	5	4	14	Not good enough in viva-voce
6	Design and realization of an 8 bit parallel load and serial out shift register using flip-flops	6-9-2019	5	5	5	15	Improper connection
					Average	14	

Faculty Member

HOD

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Department of Electronics and Communication Engineering

Academic Year: 2019-20 | II B. Tech | Semester: II | Internal -I | Section-A

Day to Day Lab Evaluation

Name of the Lab: DSD LAB
Roll No.: 18QM1A0404

Name of the Student: AdidhodlaNagalakshmi

S. No.	Name of the Experiment	Date of Experiment	Record of previous experiment (5 marks)	Execution of experiment (5 marks)	Viva-voce (5 marks)	Total (15 marks)	Remarks by Faculty
1	Realization of Boolean Expressions using Gates	9-8-2019	5	5	4	14	Not good enough in viva-voce
2	Design and realization logic gates using universal gates	23-8-2019	4	5	5	14	Late submission
3	Generation of clock using NAND / NOR gates	30-8-2019	5	5	5	15	Good in laboratory work
4	Design a 4 – bit Adder / Subtractor	30-8-2019	3	5	5	13	In correct graph work & not good enough
5	Design and realization of a 4 – bit gray to Binary and Binary to Gray Converter	6-9-2019	5	5	4	14	Not good enough in viva-voce
6	Design and realization of an 8 bit parallel load and serial out shift register using flip-flops	6-9-2019	5	5	5	15	Good in laboratory work
					Average	14	

Faculty Member

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Academic Year: 2019-20

Department of Electronics and Communication Engineering

II B. Tech Semester: II Internal -I Section-A

Day to Day Lab Evaluation

Name of the Lab: DSD LAB
Roll No.: 18QM1A0408

Name of the Student: Angajala Rahul

S. No.	Name of the Experiment	Date of Experiment	Record of previous experiment (5 marks)	Execution of experiment (5 marks)	Viva-voce (5 marks)	Total (15 marks)	Remarks by Faculty
1	Realization of Boolean Expressions using Gates	9-8-2019	4	4	2	10	Performance is well but not good in execution
2	Design and realization logic gates using universal gates	9-8-2019	4	3	3	10	Performance is well but not good in execution
3	Generation of clock using NAND / NOR gates	23-8-2019	4	4	1	9	Performance is well but not good in execution
4	Design a 4 – bit Adder / Subtractor	30-8-2019	4	4	2	10	Performance is well but not good in execution
5	Design and realization of a 4 – bit gray to Binary and Binary to Gray Converter	6-9-2019	4	4	3	11	Performance is well but not good in execution
6	Design and realization of an 8 bit parallel load and serial out shift register using flip-flops	6-9-2019	4	4	2	10	Performance is well but not good in execution
					Average	10	

Faculty Member

HOD

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DEPARTMENT

OF

ELECTRONICS AND COMMUNICATION ENGINEERING

NAME OF THE LABORATORY	**:**	**MICROWAVE ENGINEERING**
YEAR AND SEM	:	**IV B.TECH I SEM**
REGULATION/LAB CODE	:	**R16/ EC704PC**

MICROWAVE ENGINEERING LABORATORY MANUAL

HOD **PRINCIPAL**

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DEPARTMENT VISION

To be recognized as a full-fledged center for learning and research in various fields of Electronics and Communication Engineering through industrial collaboration and to provide consultancy for solving the real time socio-economic problems.

DEPARTMENT MISSION

- To provide innovative teaching and learning in the contemporary technologies in Electronics and Communication Engineering to support the professional aspirations of the students.
- To promote innovation through research and development among faculty and students by providing opportunities for inter-disciplinary learning in collaboration with industry.
- To encourage professional development of students that will inculcate ethical values and leadership skills while working with the community to address societal issues.

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Program Outcomes(PO's):

A graduate of the Electronics and Communication Engineering Program will demonstrate:

PO1: **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2: **Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6: **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: **Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one"s own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: **Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Educational Objectives (PEO's):

- **PEO 1:** To be equipped with skills for solving complex real-world problems related to VLSI, Embedded Systems, Signal/Image processing, and Digital and Wireless Communication.
- **PEO 2:** To develop professional skills that will equip them to succeed in their careers and encourage lifelong learning in advanced areas of Electronics and communications and related fields.
- **PEO 3:** To communicate effectively, work collaboratively and exhibit high levels of professionalism, moral and ethical responsibility.
- **PEO 4:** To develop the ability to understand and analyze engineering issues in a broader perspective with ethical responsibility towards sustainable development.

Program Specific Outcomes(PSO's)

- **PSO 1: Problem Solving Skills –** Graduates will be able to apply their knowledge in emerging electronics and communication engineering techniques to design solutions and solve complex engineering problems.
- **PSO 2: Professional Skills –** Graduate will be able to think critically, communicate effectively, and collaborate in teams through participation in co and extra-curricular activities.
- **PSO 3: Successful Career –** Graduates will possess a solid foundation in Electronics and Communications engineering that will enable them to grow in their profession and pursue lifelong learning through post-graduation and professional development.
- **PSO 4: Society Impact –** Graduate will be able to work with the community and collaborate to develop technological solutions that would promote sustainable development in the society.

KG REDDY College of Engineering & Technology

Syllabus of Microwave Engineering Lab

B.Tech. IV Year I Sem.

Regulation: R16 **L T P C**

Subject: MICROWAVE ENGINEERING LAB **0 0 3 2**

Course Code: EC704PC

Note: Minimum of 12 experiments to be conducted

1. Reflex Klystron Characteristics
2. Gunn Diode Characteristics
3. Directional Coupler Characteristics
4. VSWR Measurement of Matched load
5. VSWR measurement of with open and short circuit loads
6. Measurement of Waveguide Parameters
7. Measurement of Impedance of a given Load
8. Measurement of Scattering Parameters of a E plane Tee
9. Measurement of Scattering Parameters of a H plane Tee
10. Measurement of Scattering Parameters of a Magic Tee
11. Measurement of Scattering Parameters of a Circulator
12. Attenuation Measurement
13. Microwave Frequency Measurement
14. Antenna Pattern Measurements.

Course Outcomes (CO's)

Upon completion of this course, the student will be able to:

- Utilize Microwave bench to measure S Parameters of microwave Junctions
- Utilize Microwave bench to measure waveguide parameters like Wavelength, frequency, VSWR, attenuation
- Utilize Microwave bench to find the characteristics of Klystron Oscillator, Gunn diode.
- Utilize a microwave test bench for finding Radiation pattern of Horn antenna.

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Safety instructions of Microwave Lab

1. Use of Fire extinguisher during hazards.
2. Electrical safety with proper earthing.
3. Use of Insulated tools
4. Use of cooling fan to avoid damage of equipment(s).
5. Use of Proper footwear to avoid electrical shocks
6. Avoid use of improperly earthed equipments.
7. Operate the equipments within operating range.
8. Medical first aid kit.
9. Use of proper clothing with apron.
10. Exhaust fans are provided in labs for improving air quality and ventilation

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INSTRUCTIONS FOR STUDENTS (DOs & DONTs)

These are the instructions for the students attending the lab :

- ✓ Before entering the lab the student should carry the following things (MANDATORY)
  - ➢ Identity card issued by the college.
  - ➢ Class notes
  - ➢ Lab observation book
  - ➢ Lab Manual
  - ➢ Lab Record
- ✓ Student must sign in and sign out in the register provided when attending the lab session without fail.
- ✓ Come to the laboratory in time. Students, who are late more than 15 min., will not be allowed to attend the lab.
- ✓ Students need to maintain 100% attendance in lab if not a strict action will be taken.
- ✓ All students must follow a Dress Code while in the laboratory
- ✓ Foods, drinks are NOT allowed.
- ✓ All bags must be left at the indicated place.
- ✓ Refer to the lab staff if you need any help in using the lab.
- ✓ Respect the laboratory and its other users.
- ✓ Workspace must be kept clean and tidy after experiment is completed.
- ✓ Read the Manual carefully before coming to the laboratory and be sure about what you are supposed to do.
- ✓ Do the experiments as per the instructions given in the manual.
- ✓ Copy all the programs to observation which are taught in class before attending the lab session.
- ✓ Students are not supposed to use floppy disks, pen drives without permission of lab- in charge.
- ✓ Lab records need to be submitted on or before the date of submission.

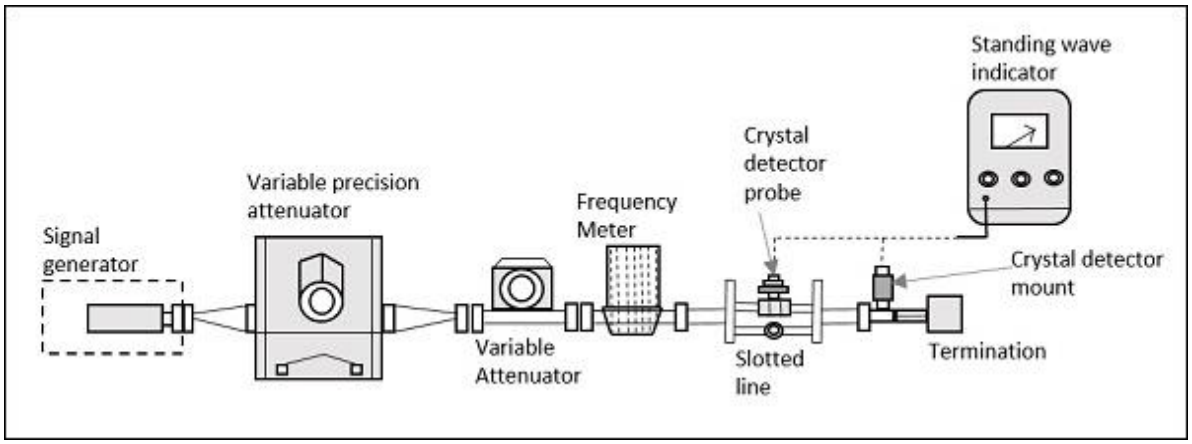
INTRODUCTION TO THE MICROWAVE ENGINEERING LAB

Microwaves are the waves having a frequency range from 1GHz to 1000GHz. They have following advantages:

1. Increased bandwidth availability
2. Improved directive properties
3. Less Fading effect and more reliability
4. Low Power required at transmitter and receiver
5. They have transparency property

Microwave Bench General Measurement Setup

This setup is a combination of different parts which can be observed in detail. The following figure clearly explains the setup.



Signal Generator

As the name implies, it generates a microwave signal, in the order of a few milliwatts. This uses velocity modulation technique to transfer continuous wave beam into milliwatt power.

A Gunn diode oscillator or a Reflex Klystron tube could be an example for this microwave signal generator.

Precision Attenuator

This is the attenuator which selects the desired frequency and confines the output around 0 to 50db. This is variable and can be adjusted according to the requirement.

Variable Attenuator

This attenuator sets the amount of attenuation. It can be understood as a fine adjustment of values, where the readings are checked against the values of Precision Attenuator.

Isolator

This removes the signal that is not required to reach the detector mount. Isolator allows the signal to pass through the waveguide only in one direction.

Frequency Meter

This is the device which measures the frequency of the signal. With this frequency meter, the signal can be adjusted to its resonance frequency. It also gives provision to couple the signal to waveguide.

Crystal Detector

A crystal detector probe and crystal detector mount are indicated in the above figure, where the detector is connected through a probe to the mount. This is used to demodulate the signals.

Standing Wave Indicator

The standing wave voltmeter provides the reading of standing wave ratio in dB. The waveguide is slotted by some gap to adjust the clock cycles of the signal. Signals transmitted by waveguide are forwarded through BNC cable to VSWR or CRO to measure its characteristics.

Slotted Line

In a microwave transmission line or waveguide, the electromagnetic field is considered as the sum of incident wave from the generator and the reflected wave to the generator. The reflections indicate a mismatch or a discontinuity. The magnitude and phase of the reflected wave depends upon the amplitude and phase of the reflecting impedance.

The standing waves obtained are measured to know the transmission line imperfections which is necessary to have a knowledge on impedance mismatch for effective transmission. This slotted line helps in measuring the standing wave ratio of a microwave device.

Construction

The slotted line consists of a slotted section of a transmission line, where the measurement has to be done. It has a travelling probe carriage, to let the probe get connected wherever necessary, and the facility for attaching and detecting the instrument.

In a waveguide, a slot is made at the center of the broad side, axially. A movable probe connected to a crystal detector is inserted into the slot of the waveguide.

Operation

The output of the crystal detector is proportional to the square of the input voltage applied. The movable probe permits convenient and accurate measurement at its position. But, as the probe is moved along, its output is proportional to the standing wave pattern, which is formed inside the waveguide. A variable attenuator is employed here to obtain accurate results.

The output VSWR can be obtained by

$VSWR=\sqrt{(V_{max}/V_{min})}$

In order to obtain a low frequency modulated signal on an oscilloscope, a slotted line with a tunable detector is employed. A slotted line carriage with a tunable detector can be used to measure the following.

- VSWR (Voltage Standing Wave Ratio)
- Standing wave pattern
- Impedance
- Reflection coefficient
- Return loss
- Frequency of the generator used

Tunable Detector

The tunable detector is a detector mount which is used to detect the low frequency square wave modulated microwave signals. The following figure gives an idea of a tunable detector mount.

To provide a match between the Microwave transmission system and the detector mount, a tunable stub is often used. There are three different types of tunable stubs.

- Tunable waveguide detector
- Tunable co-axial detector
- Tunable probe detector

Also, there are fixed stubs like −

- Fixed broad band tuned probe

- Fixed waveguide matched detector mount

The **Detector mount** is the final stage on a Microwave bench which is terminated at the end.

A microwave bench set up in real-time application would look as follows −

KG REDDY College of Engineering & Technology

CONTENTS

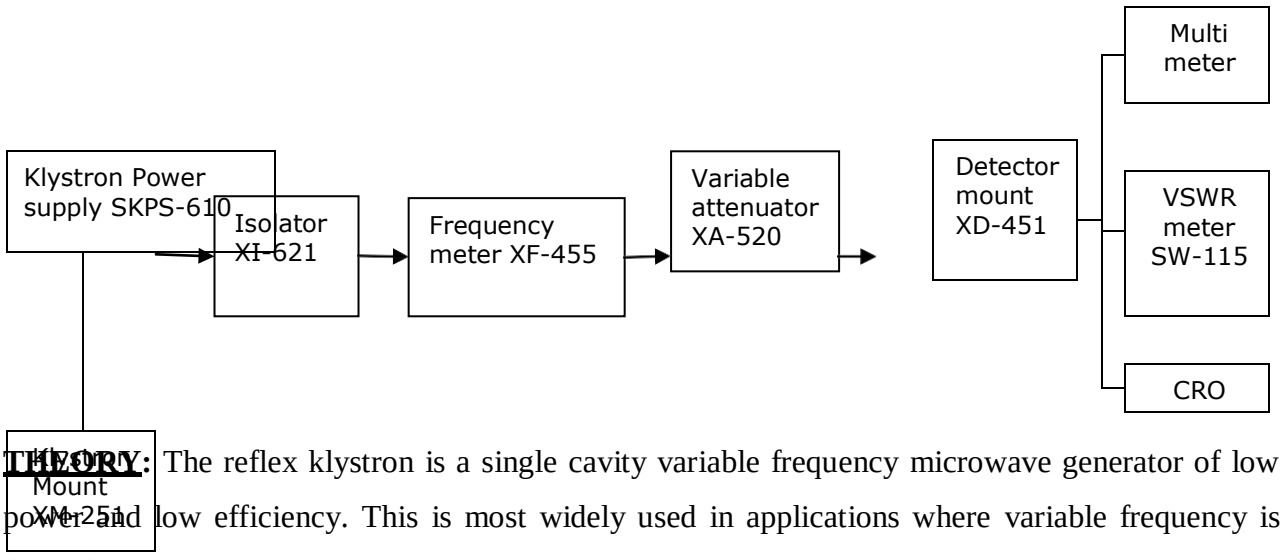
Experiment -1

REFLEX KLYSTRON CHARACTERISTICS

AIM: To study the mode characteristics of the reflex klystron tube and to determine its electronic tuning range.

EQUIPMENT REQUIRED:

1. Klystron power supply – {SKPS – 610 }
2. Klystron tube 2k-25 with klystron mount – {XM-251}
3. Isolator {X_1-625}
4. Frequency meter {XF-710}
5. Detector mount {XD-451}
6. Variable Attenuator {XA-520}
7. Wave guide stand {XU-535}
8. VSWR meter {SW-215}
9. Oscilloscope
10. BNC Cable Block Diagram:



THEORY: The reflex klystron is a single cavity variable frequency microwave generator of low power and low efficiency. This is most widely used in applications where variable frequency is desired as

1. In radar receivers
2. Local oscillator in μw receivers
3. Signal source in micro wave generator of variable frequency
4. Portable micro wave links.
5. Pump oscillator in parametric amplifier

Voltage Characteristics: Oscillations can be obtained only for specific combinations of anode and repeller voltages that gives farable transit time.

Power Output Characteristics: The mode curves and frequency characteristics. The frequency of resonance of the cavity decides the frequency of oscillation. A variation in repeller voltages slightly changes the frequency.

EXPERIMENTAL PROCEDURE:

A. CARRIER WAVE OPERATION:

1. Connect the equipments and components as shown in the figure.
2. Set the variable attenuator at maximum Position.
3. Set the MOD switch of Klystron Power Supply at CW position, beam voltage control knob to fully anti clock wise and reflector voltage control knob to fully clock wise and meter switch to 'OFF' position.
4. Rotate the Knob of frequency meter at one side fully.
5. Connect the DC microampere meter with detector.
6. Switch "ON" the Klystron power supply, CRO and cooling fan.
7. Put the meter switch to beam voltage position and rotate the beam voltage knob clockwise slowly up to 300 volts and observe the beam current position. The beam current should not increase more than 30 mA.
8. Change the reflector voltage slowly and watch the current meter, set the maximum voltage on CRO. If no deflection is obtained, change the multimeter knob position to μA.
9. Tune the plunger of klystron mount for the maximum output.
10. Rotate the knob of frequency meter slowly and stop at that position, where there is lowest output current on multimeter. Read directly the frequency meter between two horizontal line and vertical marker. If micrometer type frequency meter is used read the micrometer reading and find the frequency from it's frequency chart.
11. Change the reflector voltage and read the current and frequency for each reflector voltage.

B. SQUARE WAVE OPERATION:

1. Connect the equipments and components as shown in figure
2. Set Micrometer of variable attenuator around some Position.
3. Set the range switch of VSWR meter at 40 db position, input selector switch to crystal

impedance position, meter switch to narrow position.

4. Set Mod-selector switch to AM-MOD position .beam voltage control knob to fully anti clockwise position.
5. Switch "ON" the klystron power Supply, VSWR meter, CRO and cooling fan.
6. Switch "ON" the beam voltage. Switch and rotate the beam voltage knob clockwise up to 300V in meter.
7. Keep the AM – MOD amplitude knob and AM – FREQ knob at the mid position.
8. Rotate the reflector voltage knob to get deflection in VSWR meter or square wave on CRO.
9. Rotate the AM – MOD amplitude knob to get the maximum output in VSWR meter or CRO.
10. Maximize the deflection with frequency knob to get the maximum output in VSWR meter or CRO.
11. If necessary, change the range switch of VSWR meter 30dB to 50dB if the deflection in VSWR meter is out of scale or less than normal scale respectively. Further the output can be also reduced by variable attenuator for setting the output for any particular position.

C. MODE STUDY ON OSCILLOSCOPE:

1. Set up the components and equipments as shown in Fig.
2. Keep position of variable attenuator at min attenuation position.
3. Set mode selector switch to FM-MOD position FM amplitude and FM frequency knob at mid position keep beam voltage knob to fully anti clock wise and reflector voltage knob to fully clockwise position and beam switch to 'OFF' position.
4. Keep the time/division scale of oscilloscope around 100 HZ frequency measurement and volt/div. to lower scale.
5. Switch 'ON' the klystron power supply and oscilloscope.
6. Change the meter switch of klystron power supply to Beam voltage position and set beam voltage to 300V by beam voltage control knob.
7. Keep amplitude knob of FM modulator to max. Position and rotate the reflector voltage anti clock wise to get the modes as shown in figure on the oscilloscope. The horizontal axis represents reflector voltage axis and vertical represents o/p power.
8. By changing the reflector voltage and amplitude of FM modulation in any mode of klystron tube can be seen on oscilloscope.

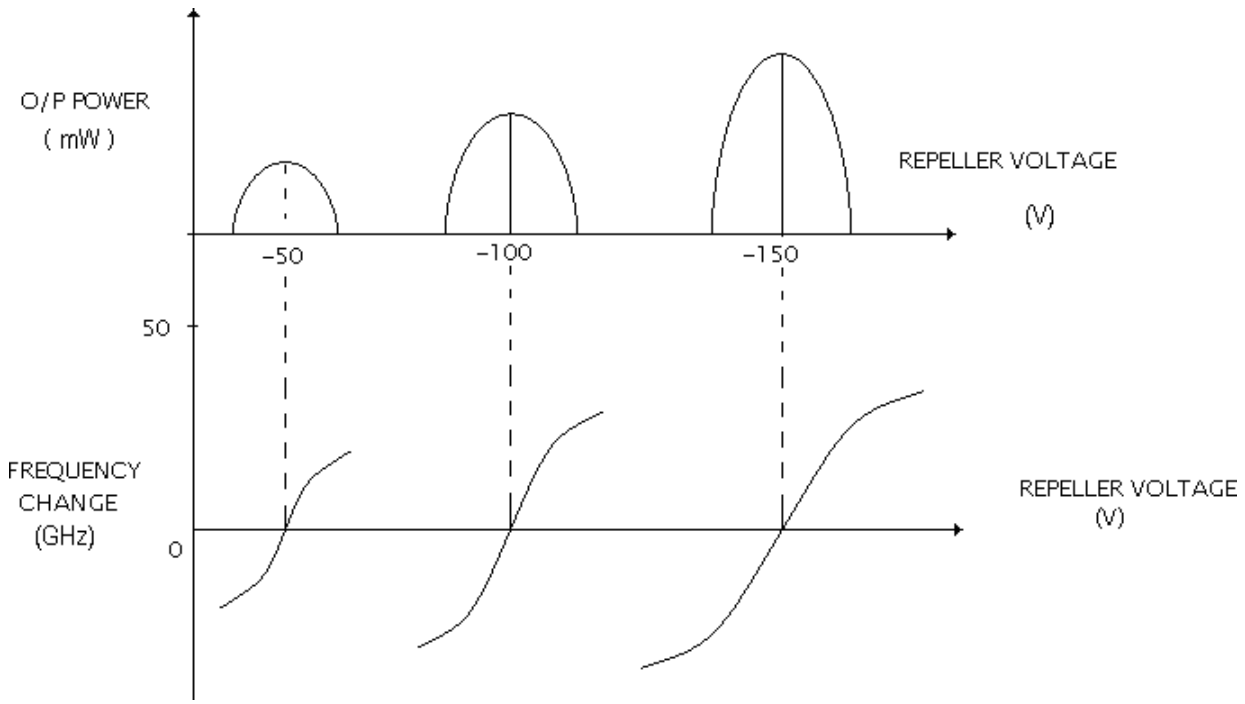
OBSERVATION TABLE:

Beam Voltage.....V (Constant)

Beam Current .....mA

Repeller Voltage (V)	Amplitude (mV)	Power (mW)	Dip Frequency (GHz)

EXPECTED GRAPH;



RESULT:

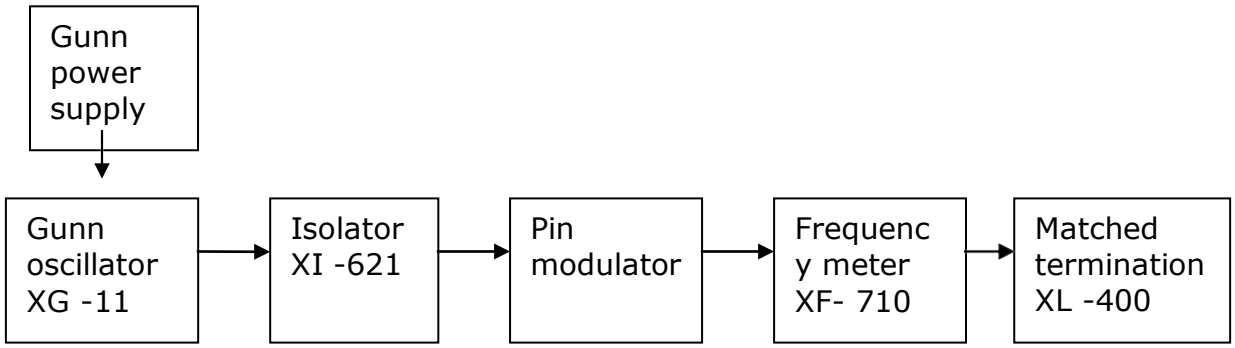
EXPERIMENT -2
GUNN DIODE CHARACTERISTICS

AIM: To study the V-I characteristics of Gunn diode.

EQUIPMENT REQUIRED:

1. Gunn power supply
2. Gunn oscillator
3. PIN Modulator
4. Isolator
5. Frequency Meter
6. Variable attenuator
7. Slotted line
8. Detector mount and CRO.

BLOCK DIAGRAM



THEORY: Gunn diode oscillator normally consist of a resonant cavity, an arrangement for coupling diode to the cavity a circuit for biasing the diode and a mechanism to couple the RF power from cavity to external circuit load. A co-axial cavity or a rectangular wave guide cavity is commonly used.

The circuit using co-axial cavity has the Gunn diode at one end at one end of cavity along with the central conductor of the co-axial line. The O/P is taken using a inductively or capacitively coupled probe. The length of the cavity determines the frequency of oscillation. The location of the coupling loop or probe within the resonator determines the load impedance presented to the Gunn diode. Heat sink conducts away the heat due to power dissipation of the device.

PROCEDURE:

1. Set the components and equipments as shown in Figure 1.
2. Initially set the variable attenuator for maximum attenuation.
3. Keep the control knobs of Gunn power supply as below

   Meter switch – "OFF"

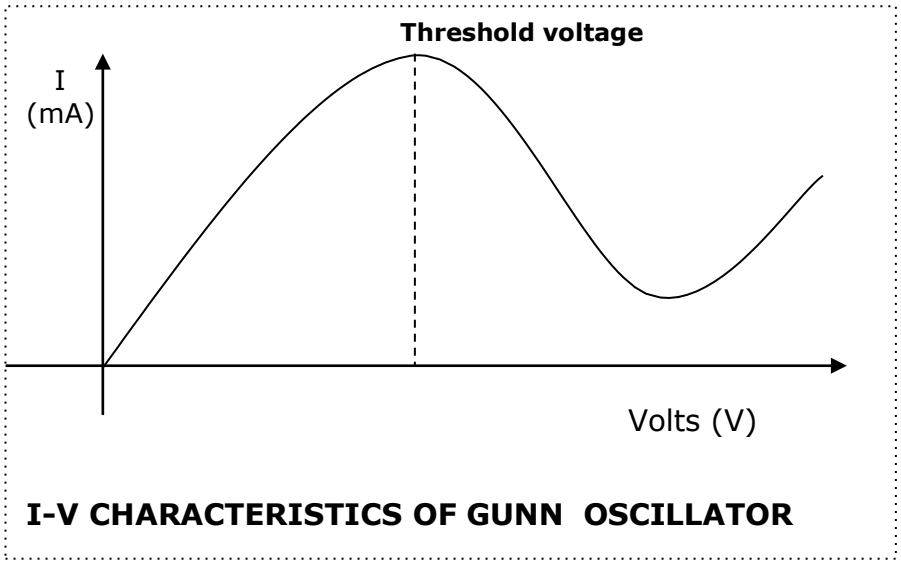
   Gunn bias knob – Fully anti clock wise

   PIN bias knob – Fully anti clock wise

   PIN mode frequency – any position
4. Set the micrometer of Gunn oscillator for required frequency of operation.
5. Switch "ON" the Gunn power supply.
6. Measure the Gunn diode current to corresponding to the various Gunn bias voltage through the digital panel meter and meter switch. Do not exceed the bias voltage above 10 volts.
7. Plot the voltage and current reading on the graph as shown in figure 2.
8. Measure the threshold voltage which corresponding to max current.

Note: Do not keep Gunn bias knob position at threshold position for more than 10-15 sec. readings should be obtained as fast as possible. Otherwise due to excessive heating Gunn diode may burn

EXPECTED GRAPH:



I-V CHARACTERISTICS OF GUNN OSCILLATOR

OBSERVATION TABLE:

Gunn bias voltage (v)	Gunn diode current (mA)

RESULT:

EXPERIMENT - 3
DIRECTIONAL COUPLER CHARACTERISTICS

AIM: To study the function of multi-hole directional coupler by measuring the following parameters.

1. The coupling factor, Insertion Loss and directivity of the coupler

EQUIPMENT REQUIRED:

1. Microwave Source (Klystron or Gunn-Diode)
2. Isolator, Frequency Meter
3. Variable Attenuator
4. Slotted Line
5. Tunable Probe
6. Detector Mount Matched Termination
7. MHD Coupler
8. Waveguide Stand
9. Cables and Accessories
10. CRO.

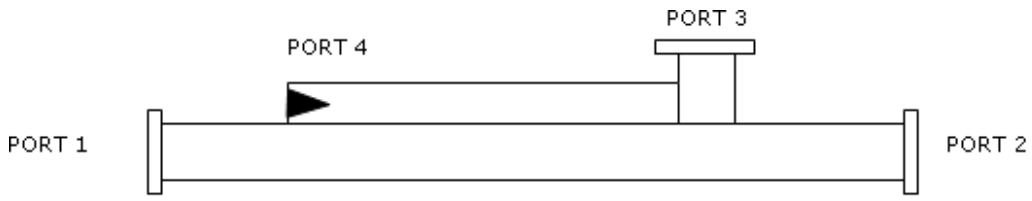


FIG. DIRECTIONAL COUPLER

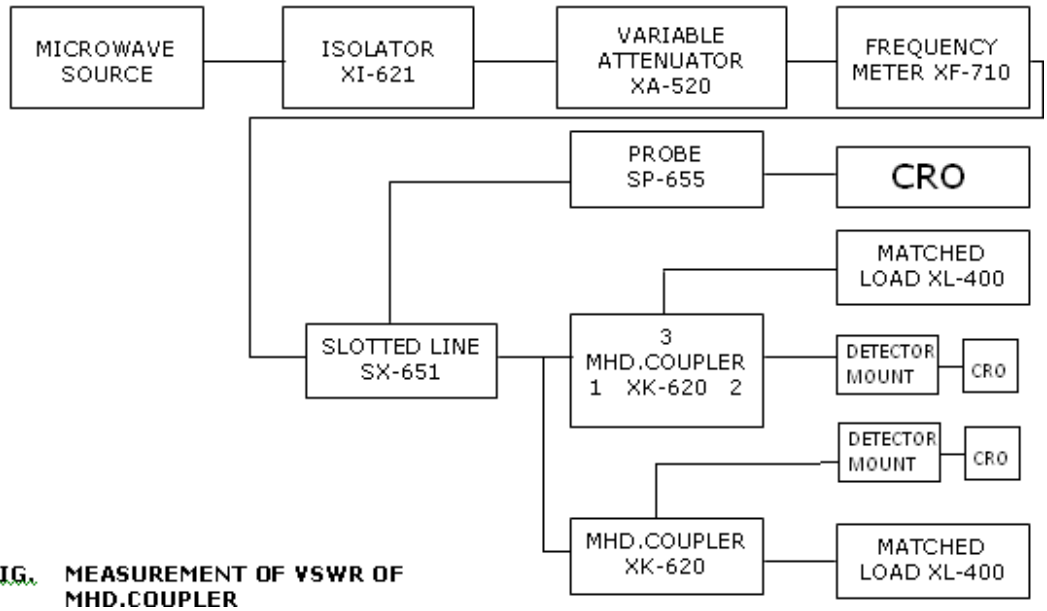


FIG. MEASUREMENT OF VSWR OF MHD.COUPLER

THEORY:

A directional coupler is a device with which it is possible to measure the incident and reflected wave separately. It consist of two transmission lines the main arm and auxiliary arm, electromagnetically coupled to each other Refer to the Fig.1. The power entering, in the main-arm gets divided between port 2 and 3, and almost no power comes out in port (4) Power entering at port 2 is divided between port 1 and 4.

The coupling factor is defined as

Coupling (db) = 10 $\log_{10}$ [P1/P3] where port 2 is terminated, Isolation (dB) = 10 $\log_{10}$ [P2/P3] where P1 is matched.

With built-in termination and power entering at Port 1, the directivity of the coupler is a measure of separation between incident wave and the reflected wave. Directivity is measured indirectly as follows:

Hence Directivity D (db) = I-C = 10 $\log_{10}$ [P2/P1]

Main line VSWR is SWR measured, looking into the main-line input terminal when the matched loads are placed at all other ports.

Auxiliary live VSWR is SWR measured in the auxiliary line looking into the output terminal when the matched loads are placed on other terminals.

Main line insertion loss is the attenuation introduced in the transmission line by insertion of coupler, it is defined as:

Insertion Loss (dB) = 10 $\log_{10}$ [P1/P2]

PROCEDURE:

1. Set up the equipments as shown in the Fig.
2. Energize the microwave source for particular operation of frequency.
3. Remove the multi hold directional coupler and connect the detector mount to the slotted section.
4. Set maximum amplitude in CRO with the help of variable attenuator let it be X.
5. Insert the directional coupler between slotted line and detector mount keeping port 1 to slotted line detector mount to the auxiliary port 3 and matched termination to port 2 without changing the position of variable attenuator.
6. Note down the amplitude using CRO let it be Y.
7. Calculate the coupling factor X-Y in dB.
8. Now carefully disconnect the detector mount form the auxiliary port 3 and matched termination

from port 2 , without disturbing the setup.

9. Connect the matched termination to the auxiliary port 3 and detector to port 2 and measure the amplitude on CRO .let it be Z
10. Repeat the steps from 1 to 4.
11. Connect the directional coupler in the reverse direction i.e., port 2 to slotted section matched termination to port 1 and detector mount to port 3 without disturbing the position of the variable attenuator.
12. Measure and note down the amplitude using CRO let it be Y_0.
13. Compute the directivity as $Y-Y_0$ in dB.

RESULT:

EXPERIMENT - 4

VSWR MEASUREMENT OF MATCHED LOAD

AIM: To determine the standing-wave ratio and reflection coefficient.

EQUIPMENT REQUIRED:

1. Klystron tube (2k25)
2. Klystron power supply (SKPS - 610)
3. VSWR meter (SW 115)
4. Klystron mount (XM – 251)
5. Isolator (XF 621)
6. Frequency meter (XF 710)
7. Variable attenuator (XA – 520)
8. Slotted line (X 565)
9. Wave guide stand (XU 535)
10. Movable short/termination XL 400
11. BNC CableS-S Tuner (XT – 441)

BLOCK DIAGRAM

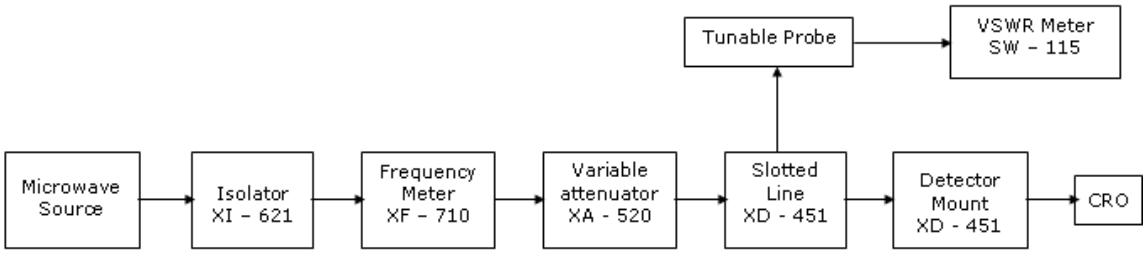


FIG: SET UP FOR LOW VSWR MEASUREMENT

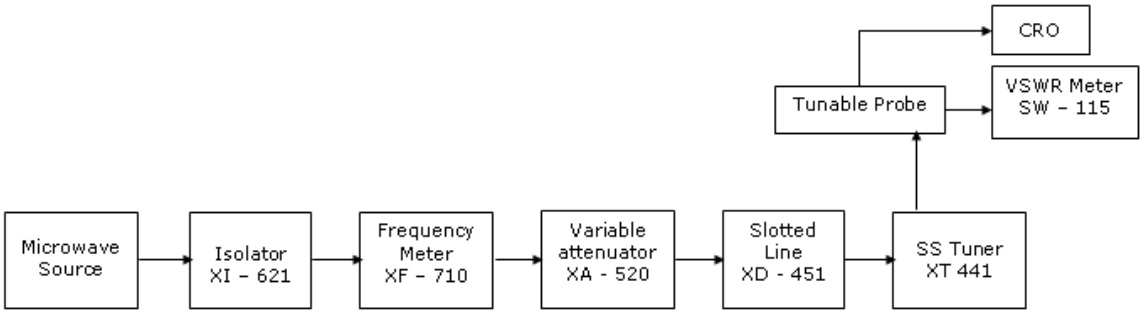


FIG: SET UP FOR HIGH VSWR MEASUREMENT

THEORY: Any mismatched load leads to reflected waves resulting in standing waves along the length of the line. The ratio of maximum to minimum voltage gives the VSWR. Hence minimum value of S is unity. If S<10 then VSWR is called low VSWR. If S>10 then VSWR is called high VSWR. The VSWR values more than 10 are very easily measured with this setup. It can be read off directly on the VSWR meter calibrated. The measurement involves simply adjusting the attenuator to give an adequate reading on the meter which is a D.C. mill volt meter. The probe on the slotted wave guide is moved t get maximum reading on the meter. The attenuation is now adjusted to get full scale reading. Next the probe on the slotted line is adjusted to get minimum, reading on the meter. The ratio of first reading to the second gives the VSWR. The meter itself can be calibrated in terms of VSWR. Double minimum method is used to measure VSWR greater than 10. In this method, the probe is inserted to a depth where the minimum can be read without difficulty. The probe is then moved to a point where the power is twice the minimum.

PROCEDURE:

1. Set up equipment as shown in figure.
2. Keep variable attenuator in minimum attenuation position.
3. Keep control knobs of VSWR meter as below

   Range dB = 40db / 50db

   Input switch = low impedance

   Meter switch = Normal

   Gain (coarse fine) = Mid position approximately
4. Keep control knobs of klystron power supply as below.

   Beam Voltage = OFF

   Mod-Switch = AM

   Beam Voltage Knob = fully anti clock wise

   Reflection voltage knob = fully clock wise

   AM-Amplitude knob = around fully clock wise

   AM frequency and amplitude knob = mid position
5. Switch ‘ON’ the klystron power supply, VSWR meter and cooling fan.
6. Switch ‘ON” the beam voltage switch position and set (down) beam voltage at 300V.
7. Rotate the reflector voltage knob to get deflection in VSWR meter.
8. Tune the O/P by turning the reflector voltage, amplitude and frequency of AM modulation.
9. Tune plunges of klystron mount and probe for maximum deflection in VSWR meter.

10. If required, change the range db-switch variable attenuator position and (given) gain control knob to get deflection in the scale of VSWR meter.
11. As your move probe along the slotted line, the deflection will change.

A. Measurement of low and medium VSWR:

1. Move the probe along the slotted line to get maximum deflection in VSWR meter.
2. Adjust the VSWR meter gain control knob or variable attenuator until the meter indicates 1.0 on normal VSWR scale.
3. Keep all the control knob as it is move the probe to next minimum position. Read the VSWR on scale.
4. Repeat the above step for change of S-S tuner probe depth and record the corresponding SWR.
5. If the VSWR is between 3.2 and 10, change the range 0dB switch to next higher position and read the VSWR on second VSWR scale of 3 to 10.

B. Measurement of High VSWR: (double minimum method)

1. Set the depth of S-S tuner slightly more for maximum VSWR.
2. Move the probe along with slotted line until a minimum is indicated.
3. Adjust the VSWR meter gain control knob and variable attenuator to obtain n a reading of 3db in the normal dB scale (0 to 10db) of VSWR meter.
4. Move the probe to the left on slotted line until full scale deflection is obtained on 0-10 db scale. Note and record the probe position on slotted line. Let it be d1.
5. Repeat the step 3 and then move the probe right along the slotted line until full scale deflection is obtained on 0-10db normal db scale. Let it be d2.
6. Replace S-S tuner and termination by movable short.
7. Measure distance between 2 successive minima positions of probe. Twice this distance is guide wave length λg.
8. Compute SWR from following equation

$$SWR = \frac{\lambda g}{\pi (d1 - d2)}$$

OBSERVATION TABLE:

LOW VSWR

VSWR = _____

HIGH VSWR

Beam Voltage (v)	x_1 (cm)	x_2 (cm)	x_1 (cm)	x_2 (cm)	Avg $(x_1-x_2) = x$ (cm)	$\lambda g=2x$ (cm)

$\lambda g =$ 6cm

d1 (cm)	d2 (cm)	d1-d2 (cm)	VSWR = $\lambda g / \pi(d1-d2)$

RESULT: .

EXPERIMENT - 5
VSWR MEASUREMENT WITH OPEN AND SHORT CIRCUIT LOADS

AIM: To determine the standing-wave ratio and reflection coefficient with open and short circuit loads

EQUIPMENT REQUIRED:

1. Klystron tube (2k25)
2. Klystron power supply (skps - 610)
3. VSWR meter (SW 115)
4. Klystron mount (XM – 251)
5. Isolator (XF 621)
6. Frequency meter (XF 710)
7. Variable attenuator (XA – 520)
8. Slotted line (X 565)
9. Wave guide stand (XU 535)
10. Movable short/termination XL 400
11. BNC Cable S-S Tuner (XT – 441)

BLOCK DIAGRAM

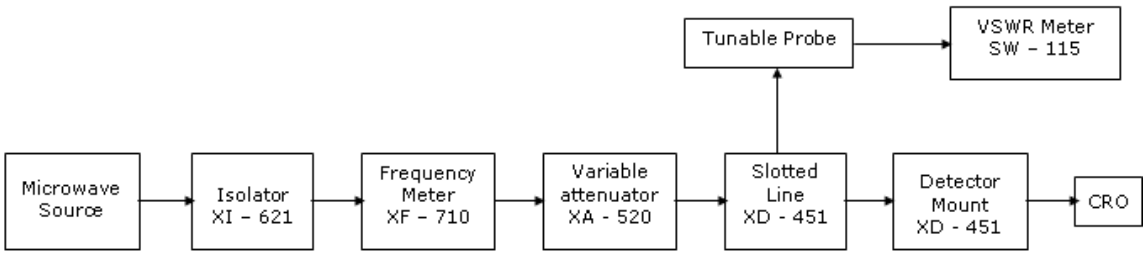


FIG: SET UP FOR LOW VSWR MEASUREMENT

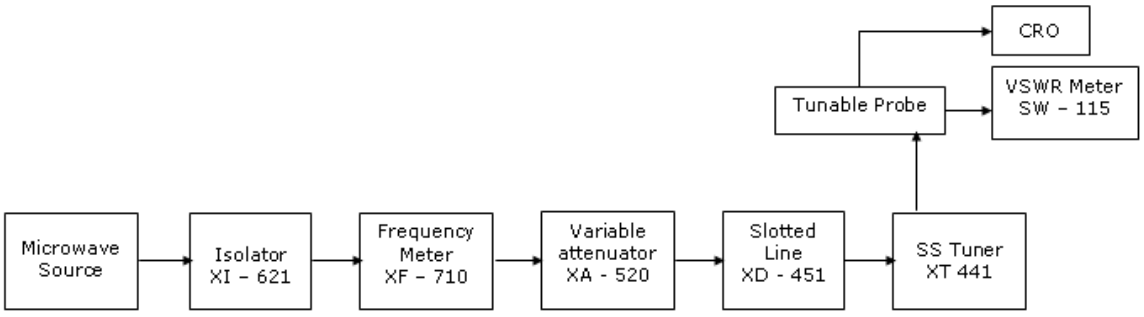


FIG: SET UP FOR HIGH VSWR MEASUREMENT

THEORY:

Any mismatched load leads to reflected waves resulting in standing waves along the length of the line. The ratio of maximum to minimum voltage gives the VSWR. Hence minimum value of S is unity. If S<10 then VSWR is called low VSWR. If S>10 then VSWR is called high VSWR. The VSWR values more than 10 are very easily measured with this setup. It can be read off directly on the VSWR meter calibrated. The measurement involves simply adjusting the attenuator to give an adequate reading on the meter which is a D.C. mill volt meter. The probe on the slotted wave guide is moved t get maximum reading on the meter. The attenuation is now adjusted to get full scale reading. Next the probe on the slotted line is adjusted to get minimum, reading on the meter. The ratio of first reading to the second gives the VSWR. The meter itself can be calibrated in terms of VSWR. Double minimum method is used to measure VSWR greater than 10. In this method, the probe is inserted to a depth where the minimum can be read without difficulty. The probe is then moved to a point where the power is twice the minimum.

PROCEDURE:

1. Set up equipment as shown in figure.
2. Keep variable attenuator in minimum attenuation position.
3. Keep control knobs of VSWR meter as below
4. Range dB = 40db / 50db Input
   switch = low impedance Meter
   switch = Normal
5. Gain (coarse fine) = Mid position approximately
6. Keep control knobs of klystron power supply as
   below. Beam Voltage = OFF
7. Mod-Switch = AM
8. Beam Voltage Knob = fully anti clock wise Reflection
   voltage knob = fully clock wise
9. AM-Amplitude knob = around fully clock wise AM
   frequency and amplitude knob = mid position
10. Switch ‘ON’ the klystron power supply, VSWR meter and cooling fan.
11. Switch ‘ON” the beam voltage switch position and set (down) beam voltage at 300V.
12. Rotate the reflector voltage knob to get deflection in VSWR meter.

13. Tune the O/P by turning the reflector voltage, amplitude and frequency of AM modulation.
14. Tune plunges of klystron mount and probe for maximum deflection in VSWR meter.
15. If required, change the range db-switch variable attenuator position and (given) gain control knob to get deflection in the scale of VSWR meter.
16. As your move probe along the slotted line, the deflection will change.

OBSERVATION TABLE:

LOW VSWR

VSWR = _____

HIGH VSWR

Beam Voltage (v)	x_1 (cm)	x_2 (cm)	x_1 (cm)	x_2 (cm)	Avg $(x_1-x_2) = x$ (cm)	$\lambda g=2x$ (cm)

$\lambda g =$ 6cm

d1 (cm)	d2 (cm)	d1-d2 (cm)	VSWR = $\lambda g / \pi(d1-d2)$

RESULT:

EXPERIMENT NO: 6

MEASUREMENT OF WAVEGUIDE PARAMETERS

AIM:

To determine the frequency and wave length in a Rectangular Waveguide working in TE10 mode.

EQUIPMENT:

1. Klystron power supply
2. Klystron tube
3. Klystron mount
4. Detector mount
5. Isolator
6. Frequency meter
7. Variable attenuator
8. Matched termination
9. Tunable probe
10. MHD coupler
11. Cooling fan
12. Slotted line
13. VSWR meter and cables
14. Wave guide stands

THEORY :

For dominant TE10 mode rectangular waveguide $\lambda 0$ λg, λc and are related as below

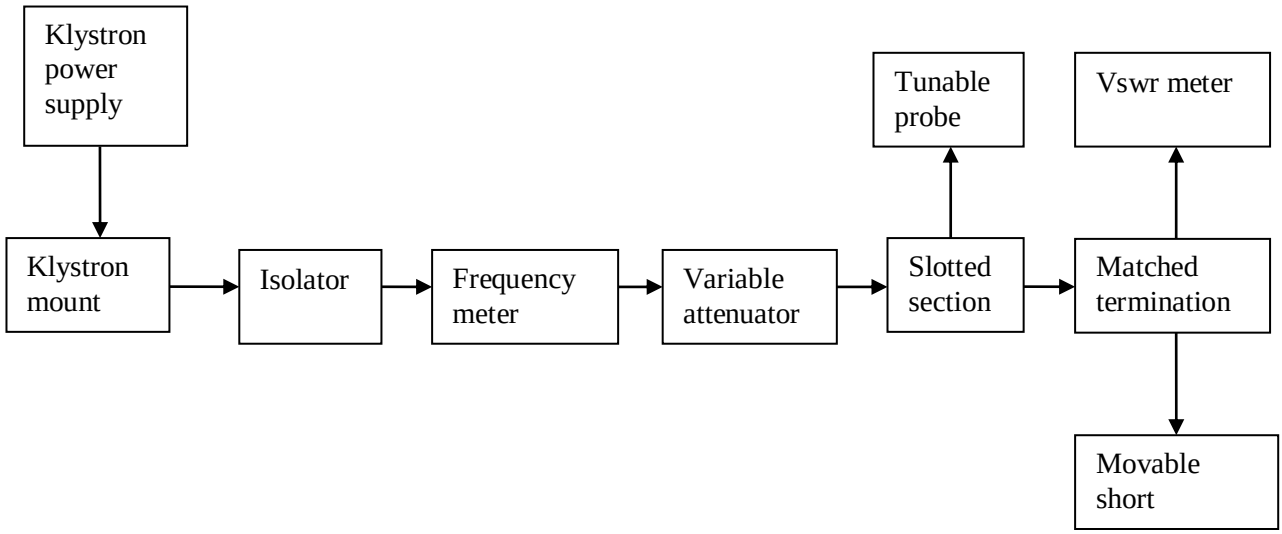
$$1/\lambda 0^2 = 1/\lambda g^2 + 1/\lambda c^2$$

$\lambda 0$ is free space wavelength

λ g is guide wavelength λ
c is cut-off wavelength
For TE10 mode = 2a where

'a' is the broader dimension of waveguide.

BLOCK DIAGRAM:



Measurement Of Waveguide Parameters

PROCEDURE

1. Set up the components and equipments as shown in figure.
2. Set up variable attenuator at minimum attenuation position.
3. Keep the control knobs of VSWR meter as below

Range - 50 dB
Input switch - crystal low impedance
Meter switch - Normal position
Gain (Coarse & fine) - Mid position

4. Keep the control knobs of klystron power supply as below

Beam voltage - OFF
Mod – switch - AM
Beam voltage knob – Fully anti-clockwise
Reflector voltage – Fully clockwise
AM-Amplitude knob - Around fully clockwise
AM-Frequency knob – Around mid-position

5. Switch on the klystron power supply, VSWR meter and cooling fan.
6. Switch on the beam voltage switch and set beam voltage at 250 volts with the help of beam voltage knob.
7. Adjust the reflector voltage to get some deflection in VSWR meter.
8. Maximize the deflection with AM amplitude and frequency control knob of power supply.
9. Tune the plunger of Klystron mount for maximum deflection.
10. Tune the reflector voltage to get some deflection in VSWR meter.

11. Tune the reflector voltage knob for maximum deflection.
12. Tune the frequency meter knob to get a dip on the VSWR scale and note down the frequency directly from frequency meter.
13. Replace the termination with movable short and detune the frequency meter.
14. Move the probe along the slotted line. The deflection in VSWR meter will vary. Move the probe to a minimum deflection position, to get accurate reading if necessary increase the VSWR meter range dB switch to higher position. Note and record the probe position.
15. Move the probe to next minimum position and record the probe position again.
16. Calculate the guide wavelength as twice the distance between two successive minimum positions obtained as above.
17. Measure the waveguide inner broad dimension 'a' which will be around 22.86 mm for X-band.
18. Calculate the frequency by following equation

$$F = c/\lambda = C\,(1/\lambda g^2 + 1/\lambda c^2)^{1/2} \text{ - Eq. Ed}$$

Where c = 3 x 10^8 meter/sec .i.e. velocity of light
19. Verify with frequency obtained by frequency meter.
20. Above experiment can be verified at different frequencies.

OBSERVATION

First minima position d1 = Second minima position d2 =

$\lambda g = 2(d1-d2) =$

Broader dimension of wave guide 'a' = 2.2 cm $\lambda c =$ 2a=

c = speed of light=3x10^8 m/s

$$F = c/\lambda = C\,(1/\lambda g^2 + 1/\lambda c^2)^{1/2}$$

Frequency reading from frequency meter =

PRECAUTIONS:

1. To protect repeller from damage the repeller negative voltage is always applied before anode voltage.
2. While modulating repeller should never become positive with respect to cavity.
3. Cooling should be provided to Reflex klystron.

RESULT:

EXPERIMENT NO: 7

MEASUREMENT OF IMPEDENCE OF A GIVEN LOAD

AIM: To measure an unknown impedance using the smith chart.

EQUIPMENT REQUIRED:

1. Klystron tube 2k25
2. Klystron power supply Skps-610
3. Klystron mount XM-251
4. Isolator XF 62
5. Frequency meter XF 710
6. Variable attenuator XA – 520
7. Slotted line XS 565
8. Tunable probe XP 655
9. VSWR meter
10. Wave guide stand SU 535
11. S-S tuner (XT 441)
12. Movable short/termination

BLOCK DIAGRAM

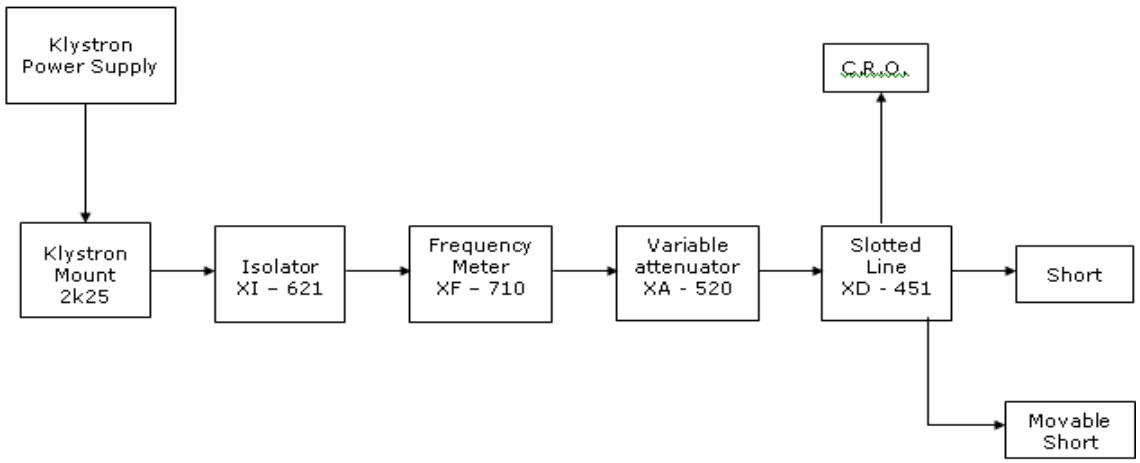


FIG: SET UP FOR IMPEDANCE MEASUREMENT

THEORY:

The impedance at any point on a transmission line can be written in the form R+jx.

For comparison SWR can be calculated as

$$S = \frac{1+|R|}{1-|R|}$$ where reflection coefficient 'R'

Given as

$$R = \frac{Z - Z_0}{Z + Z_0}$$

Z_o = characteristics impedance of wave guide at operating frequency.

Z is the load impedance

The measurement is performed in the following way.

The unknown device is connected to the slotted line and the position of one minima is determined. The unknown device is replaced by movable short to the slotted line. Two successive minima portions are noted. The twice of the difference between minima position will be guide wave length. One of the minima is used as reference for impedance measurement. Find the difference of reference minima and minima position obtained from unknown load. Let it be 'd'. Take a smith chart, taking '1' as centre, draw a circle of radius equal to S. Mark a point on circumference of smith chart towards load side at a distance equal to d/λg.

Join the center with this point. Find the point where it cut the drawn circle. The co-ordinates of this point will show the normalized impedance of load.

PROCEDURE:

1. Calculate a set of Vmin values for short or movable short as load.
2. Calculate a set of Vmin values for S-S Tuner + Matched termination as a load.

Note: Move more steps on S-S Tuner

3. From the above 2 steps calculate d = d_1~d_2
4. With the same setup as in step 2 but with few numbers of turns (2 or 3). Calculate low VSWR.

Note: High VSWR can also be calculated but it results in a complex procedure.

5. Draw a VSWR circle on a smith chart.
6. Draw a line from center of circle to impedance value (d/λg) from which calculate admittance and Reactance (Z = R±jx)

OBSERVATION TABLE:

Load (short or movable short)					
x_1 (cm)	x_2 (cm)	x_1 (cm)	x_2 (cm)	x_1 (cm)	x_2 (cm)

x = _____

Load (S.S. Tuner + Matched Termination)

λg = _____

S.S Tuner + Matched Termination	Short or Movable Short

d1= , d2 =

d = d1 ~ d2 =

Z = d/λg =

RESULT:.

EXPERIMENT 8

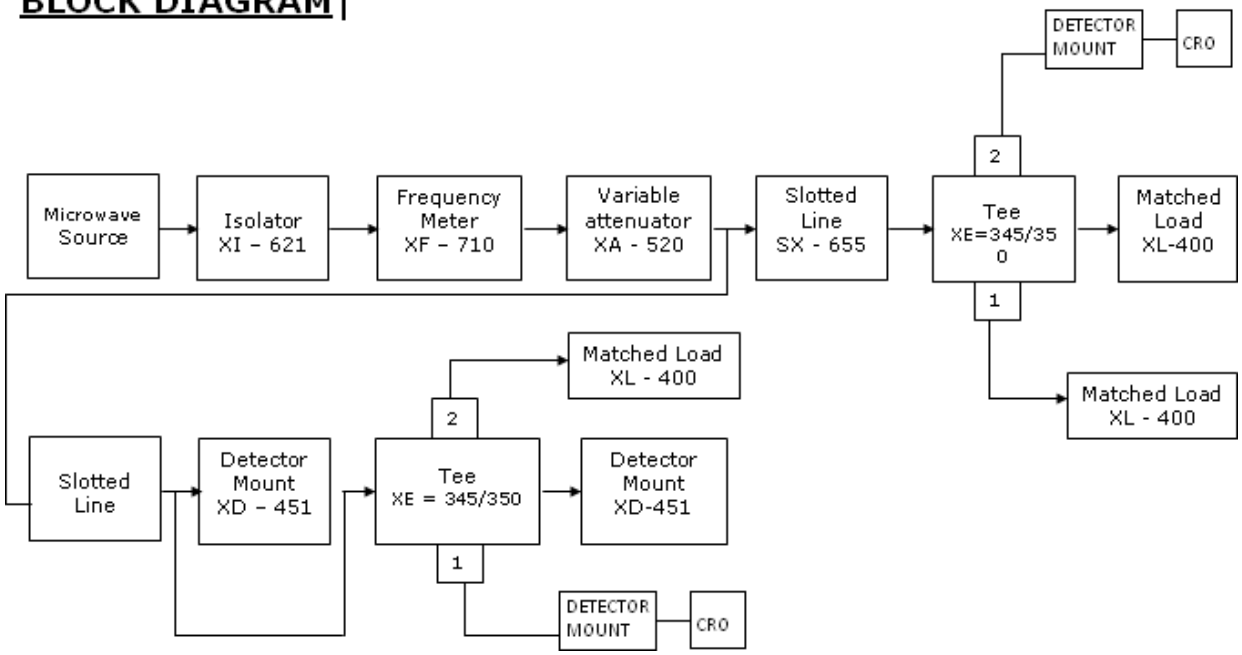
MEASURE MENT OF SCATTERING PARAMETERS OF E PLANE TEE

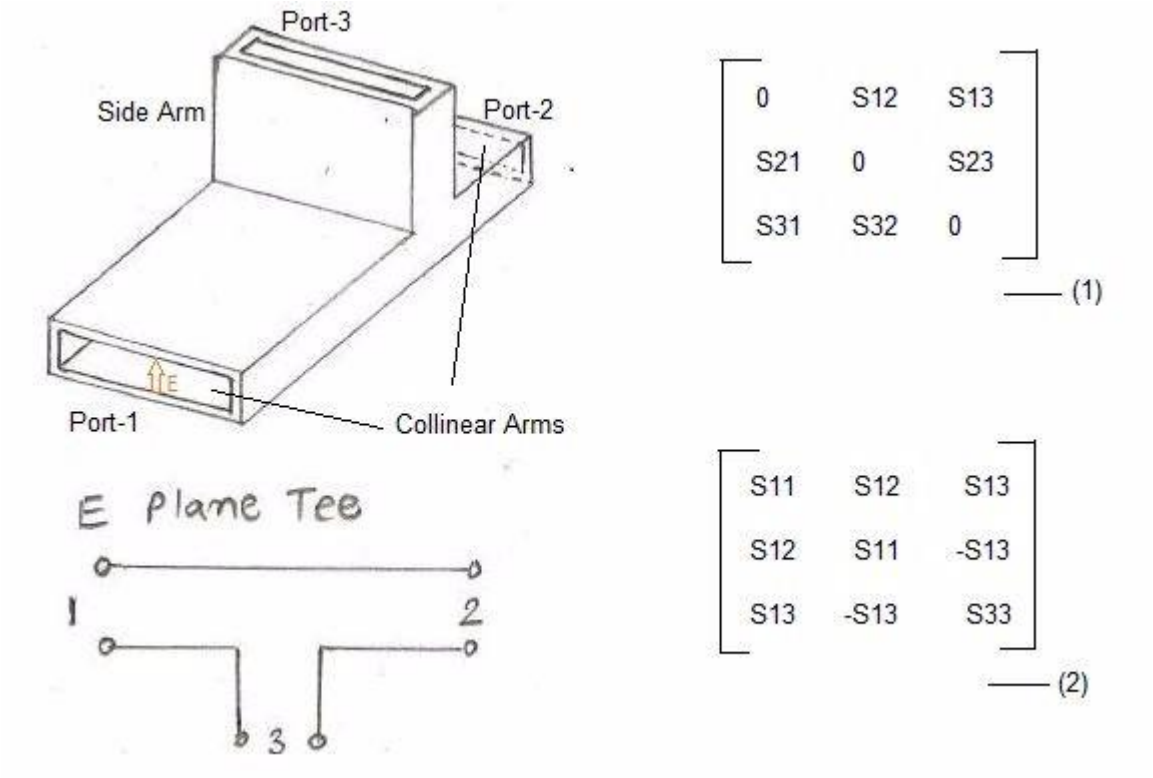
AIM: To measure of scattering parameters of E Plane Tee.

EQUIPMENT REQUIRED:

1. Microwave source : Klystron tube (2k25)
2. Isolator (XI-621)
3. Frequency meter (XF-710)
4. Variable Attenuator (XA-520)
5. Slotted line (SX-651)
6. Tunable probe (XP-655)
7. Detector Mount (XD-451)
8. Matched Termination (XL-400)
9. Magic Tee (XE-345/350)
10. Klystron Power Supply + Klystron Mount
11. Wave guide stands and accessories

BLOCK DIAGRAM





$$\begin{bmatrix} 0 & S12 & S13 \\ S21 & 0 & S23 \\ S31 & S32 & 0 \end{bmatrix} \quad \text{——— (1)}$$

$$\begin{bmatrix} S11 & S12 & S13 \\ S12 & S11 & -S13 \\ S13 & -S13 & S33 \end{bmatrix} \quad \text{——— (2)}$$

PROCEDURE:

1. Setup the components and equipments as shown in figure. Keeping E-arm towards slotted line and matched termination to other ports.
2. Energize the microwave source for particular frequency of operation and tune the detector mount for maximum output.
3. With the help of variable frequency of operation and tune the detector mount for maximum output attenuator, set any reference in the CRO let it be V_3.
4. Without disturbing the position of the variable attenuator, carefully place the magic tee after the slotted line, detector mount to E-arm and matched termination to arm-1 and arm-2.
5. Note down the amplitude using CRO let it be V_4.
6. Determine the isolation between arm-1 and arm-2 as V_3-V_4.
7. Determine the coupling co-efficient from the equation given in theory part.
8. The same experiment may be repeated for other arms also.

OBSERVATIONS:

Ports	Power (W)

PE =

PH =

RESULT:

EXPERIMENT 8

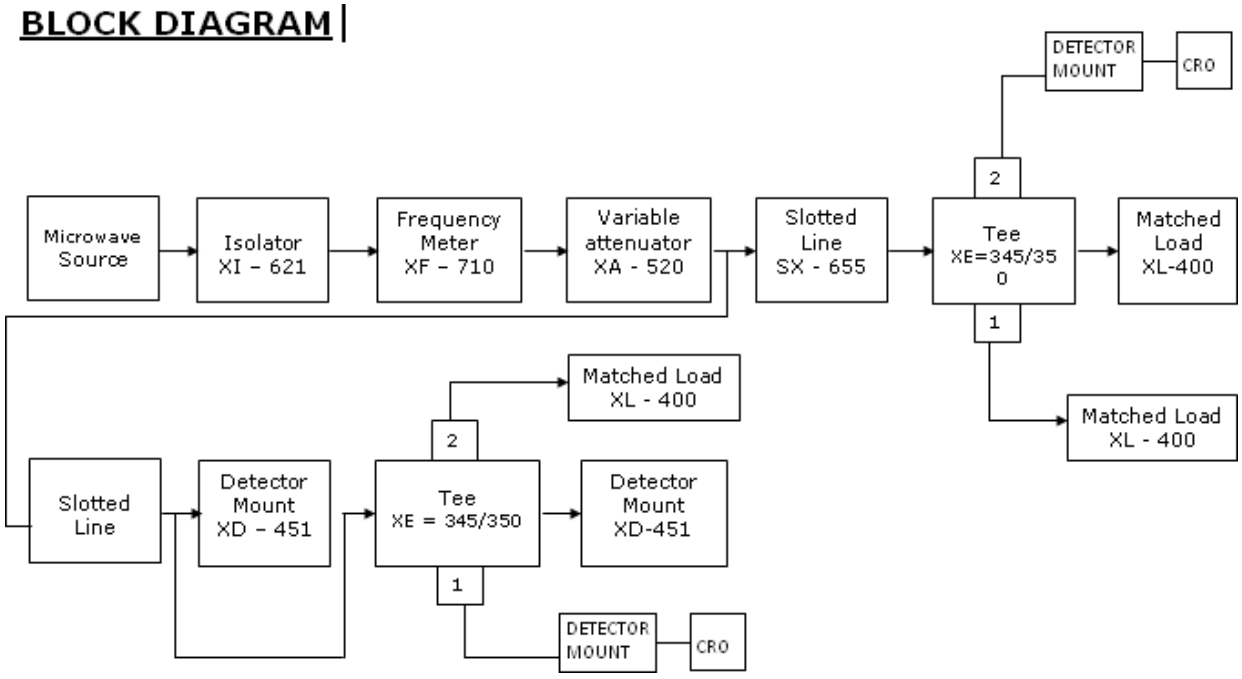
MEASURE MENT OF SCATTERING PARAMETERS OF H PLANE TEE

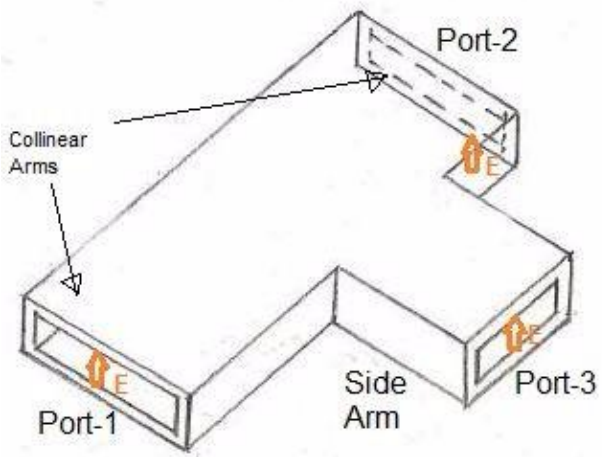
AIM: To measure of scattering parameters of H Plane Tee.

EQUIPMENT REQUIRED:

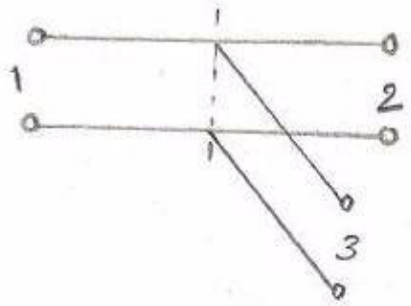
1. Microwave source : Klystron tube (2k25)
2. Isolator (XI-621)
3. Frequency meter (XF-710)
4. Variable Attenuator (XA-520)
5. Slotted line (SX-651)
6. Tunable probe (XP-655)
7. Detector Mount (XD-451)
8. Matched Termination (XL-400)
9. Magic Tee (XE-345/350)
10. Klystron Power Supply + Klystron Mount
11. Wave guide stands and accessories

BLOCK DIAGRAM





H Plane Tee



PROCEDURE:

9. Setup the components and equipments as shown in figure. Keeping E-arm towards slotted line and matched termination to other ports.
10. Energize the microwave source for particular frequency of operation and tune the detector mount for maximum output.
11. With the help of variable frequency of operation and tune the detector mount for maximum output attenuator, set any reference in the CRO let it be V_3.
12. Without disturbing the position of the variable attenuator, carefully place the magic tee after the slotted line, detector mount to E-arm and matched termination to arm-1 and arm-2.
13. Note down the amplitude using CRO let it be V_4.
14. Determine the isolation between arm-1 and arm-2 as V_3-V_4.
15. Determine the coupling co-efficient from the equation given in theory part.
16. The same experiment may be repeated for other arms also.

OBSERVATIONS:

Ports	Power (W)

PE =

PH =

RESULT:

EXPERIMENT 10

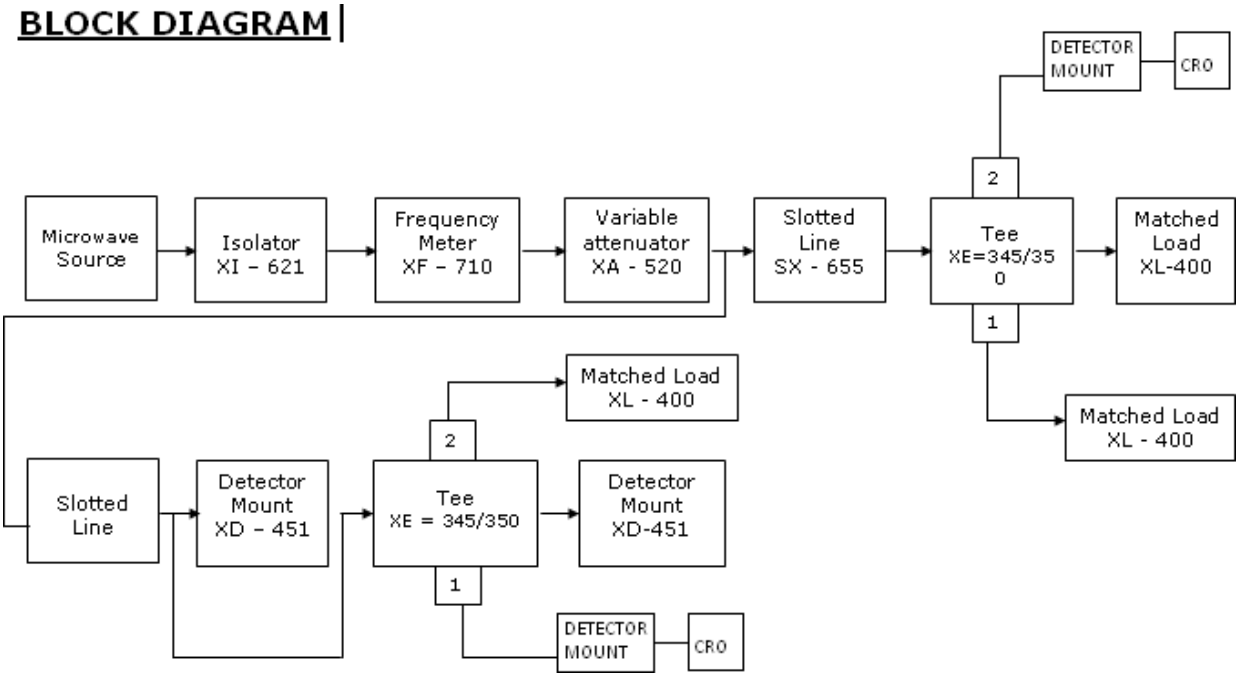
MEASURE MENT OF SCATTERING PARAMETERS OF MAGIC TEE

AIM: To measure of scattering parameters of Magic Tee.

EQUIPMENT REQUIRED:

12. Microwave source : Klystron tube (2k25)
13. Isolator (XI-621)
14. Frequency meter (XF-710)
15. Variable Attenuator (XA-520)
16. Slotted line (SX-651)
17. Tunable probe (XP-655)
18. Detector Mount (XD-451)
19. Matched Termination (XL-400)
20. Magic Tee (XE-345/350)
21. Klystron Power Supply + Klystron Mount
22. Wave guide stands and accessories

BLOCK DIAGRAM



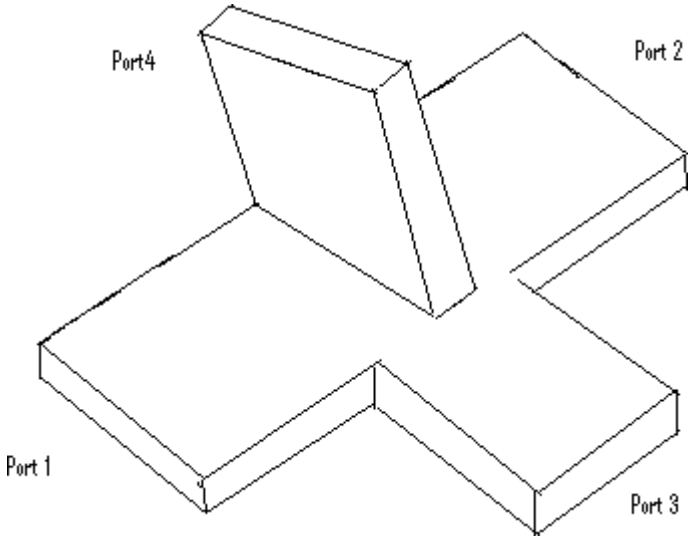


Fig: Magic Tee

THEORY:

The device Magic Tee is a combination of E and H plane Tee. Arm 3 is the H-arm and arm 4 is the E-arm. If the power is fed, into arm 3 (H-arm) the electric field divides equally between arm1 and 2 with the same phase and no electric field exists in the arm 4. If power is fed in arm 4 (E-arm) it divides equally into arm 1 and 2 but out of phase with no power to arm 3, further, if the power is fed in arm 1 and 2 simultaneously it is added in arm 3 (H-arm) and it is subtracted in E-arm i.e., arm 4.

A. Input VSWR:

Value of SWR corresponding to each port as a load to the line while other ports are terminated in matched load.

B. Isolation:

The Isolation between E and H arm is defined as the ratio of the power supplied by the generator connected to the E-arm (port 4) to the power detected at H-arm (port 3) when side arm 1 and 2 terminated in matched load.

Isolation (dB) = $10 \log_{10}$ [P4/P3]

Similarly, Isolation between other ports may be defined.

C. Coupling Factor:

It is defined as Cij = 10 – □/20

Where '□' is attenuation / isolation in dB when 'i' is input arm and 'j' is output arm.

Thus, □ = $10 \log_{10}$ [P4/P3]

Where P3 is the power delivered to arm 'i' and P4 is power detected at 'j' arm.

PROCEDURE:

1. Setup the components and equipments as shown in figure. Keeping E-arm towards slotted line and matched termination to other ports.
2. Energize the microwave source for particular frequency of operation and tune the detector mount for maximum output.
3. With the help of variable frequency of operation and tune the detector mount for maximum output attenuator, set any reference in the CRO let it be V_3.
4. Without disturbing the position of the variable attenuator, carefully place the magic tee after the slotted line, detector mount to E-arm and matched termination to arm-1 and arm-2.
5. Note down the amplitude using CRO let it be V_4.
6. Determine the isolation between arm-1 and arm-2 as V_3-V_4.
7. Determine the coupling co-efficient from the equation given in theory part.
8. The same experiment may be repeated for other arms also.

OBSERVATIONS:

Ports	Power (W)

PE =

PH =

PE-PH =

Coupling factor

PC2 =

□ = PE – PC2

CEC2 =

RESULT:

EXPERIMENT 11

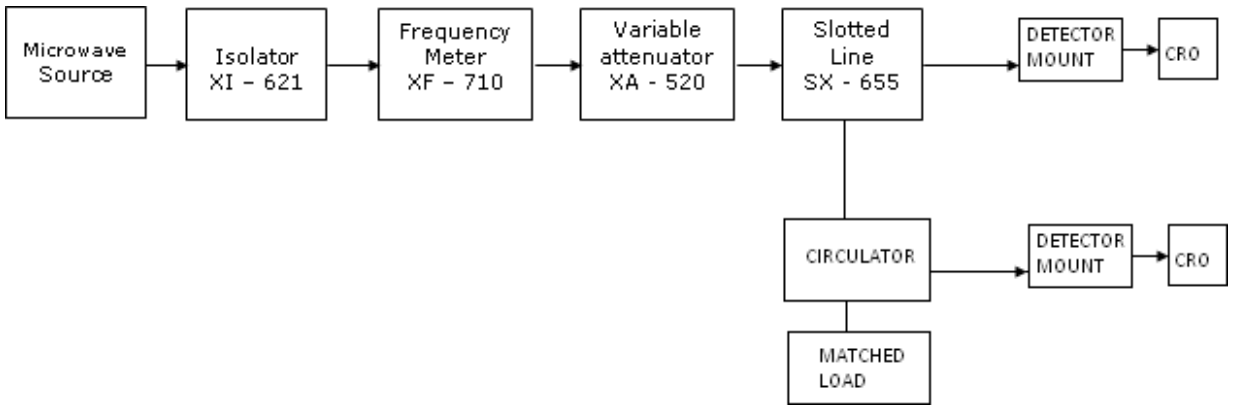
MEAUREMENT OF SCATTERING PARAMETERS OF CIRCULATOR

AIM: To measure of scattering parameters of circulator.

EQUIPMENT REQUIRED:

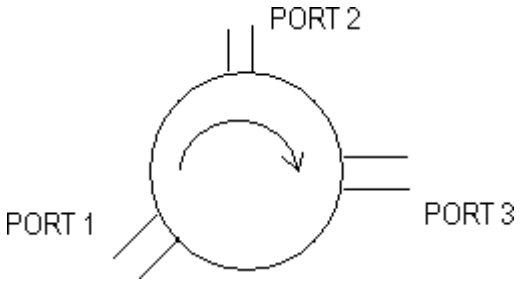
1. Microwave Source (Klystron or Gunn-Diode)
2. Isolator, Frequency Meter
3. Variable Attenuator
4. Slotted Line
5. Tunable Probe
6. Detector Mount Matched Termination
7. Circulator
8. Waveguide Stand
9. Cables and Accessories
10. VSWR Meter.

BLOCK DIAGRAM:



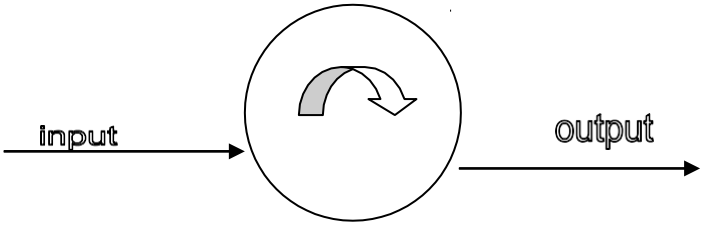
CIRCULATOR:

Circulator is defined as device with ports arranged such that energy entering a port is coupled to an adjacent port but not coupled to the other ports. This is depicted in figure circulator can have any number of ports.



ISOLATOR:

An Isolator is a two-port device that transfers energy from input to output with little attenuation and from output to input with very high attenuation.



The isolator, shown in Fig. can be derived from a three-port circulator by simply placing a matched load (reflection less termination) on one port.

The important circulator and isolator parameters are:

A. Insertion Loss

Insertion Loss is the ratio of power detected at the output port to the power supplied by source to the input port, measured with other orts terminated in the matched Load. It is expressed in dB.

B. Isolation

Isolation is the ratio of power applied to the output to that measured at the input. This ratio is expressed in db. The isolation of a circulator is measured with the third port terminated in a matched load.

C. Input VSWR

The input VSWR of an isolator or circulator is the ratio of voltage maximum to voltage minimum of the standing wave existing in the line with all parts except the test port are matched.

PROCEDURE:

Measurement of insertion loss and isolation.

1. Remove the probe and isolator or circulator from slotted line and connect the detector mount to the slotted section. The output of the detector mount should be connected with CRO.
2. Energize the microwave source for maximum output for a particular frequency of operation. Tune the detector mount for maximum output in the CRO.
3. Set any reference level of Maximum Amplitude with the help of variable attenuator, Let it be P_1.
4. Carefully remove the detector mount from slotted line without disturbing the position of the set up. Insert the isolator/circulator between slotted line and detector mount. Keep input port to slotted line and detector its output port. A matched termination should be placed at third port in case of Circulator.
5. Record the reading of Amplitude in CRO, Let it be P_2.
6. Compute insertion loss given as P_1-P_2 in db.
7. For measurement of isolation, the isolator or circulator has to be connected in reverse i.e. output port to slotted line and detector to input port with other port terminated by matched termination (for circulator).
8. Record the reading of Amplitude in CRO and let it be P_3.
9. Compute isolation as P_1-P_3 in db.
10. The same experiment can be done for other ports of circulator.
11. Repeat the above experiment for other frequency if needed.

RESULT:

EXPERIMENT 12

ATTENUATION MEASUREMENT

AIM: To study insertion loss and attenuation measurement of attenuator.

EQUIPMENT REQUIRED:

1. Microwave source Klystron tube (2k25)
2. Isolator (xI-621)
3. Frequency meter (xF-710)
4. Variable attenuator (XA-520)
5. Slotted line (XS-651)
6. Tunable probe (XP-655)
7. Detector mount (XD-451)
8. Matched termination (XL-400)
9. Test attenuator
   a) Fixed
   b) Variable
10. Klystron power supply & Klystron mount
11. Cooling fan
12. BNC-BNC cable
13. VSWR or CRO

BLOCK DIAGRAM

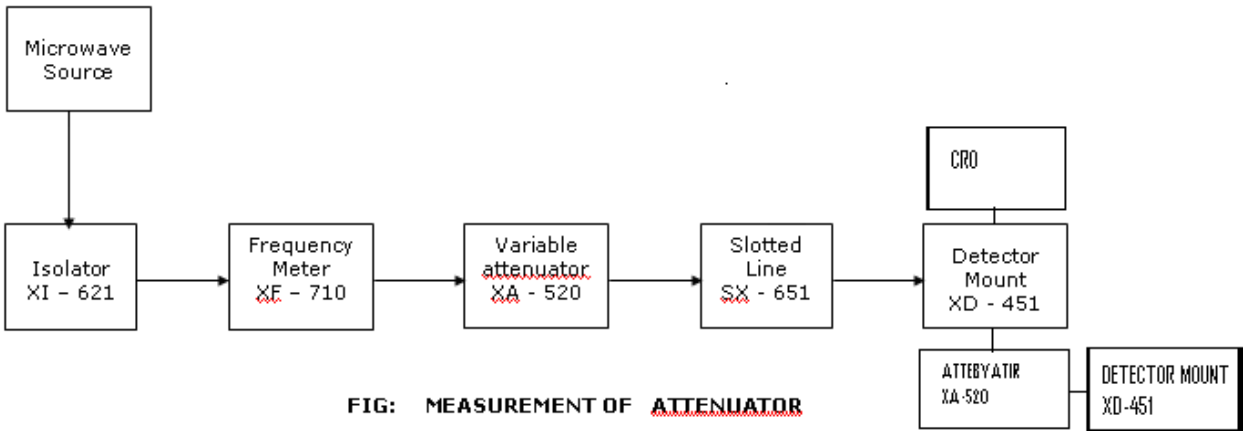


FIG: MEASUREMENT OF ATTENUATOR

THEORY:

The attenuator is a two port bidirectional device which attenuates some power when inserted into a transmission line.

Attenuation A (dB) = 10 log (P1/P2)

Where P1 = Power detected by the load without the attenuator in the line

P2 = Power detected by the load with the attenuator in the line.

PROCEDURE:

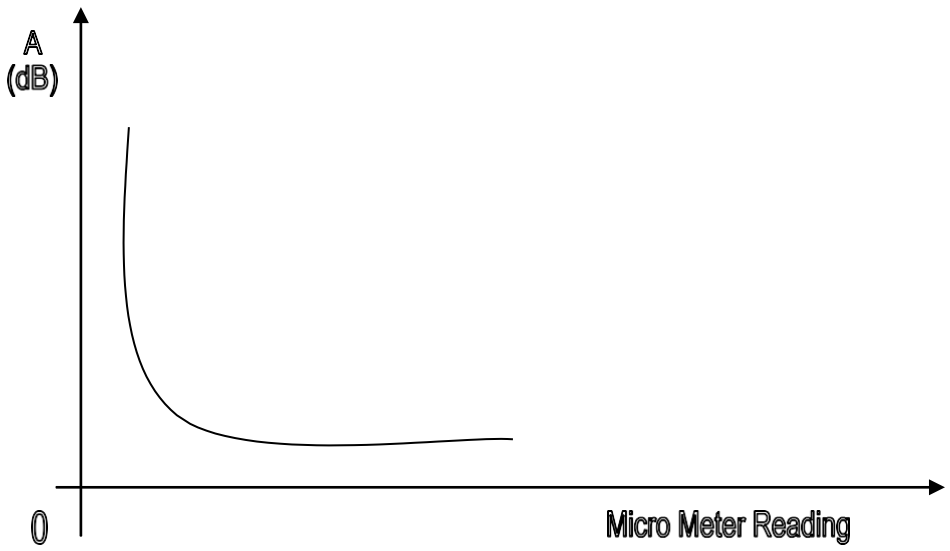
1. Connect the equipments as shown in the above figure.
2. Energize the microwave source for maximum power at any frequency of operation
3. Connect the detector mount to the slotted line and tune the detector mount also for max deflection on VSWR or on CRO
4. Set any reference level on the VSWR meter or on CRO with the help of variable attenuator. Let it be P1.
5. Carefully disconnect the detector mount from the slotted line without disturbing any position on the setup place the test variable attenuator to the slotted line and detector mount to O/P port of test variable attenuator. Keep the micrometer reading of text variable attenuator to zero and record the readings of VSWR meter or on CRO. Let it to be P2. Then the insertion loss of test attenuator will be P1-P2 db.

6. For measurement of attenuation of fixed and variable attenuator. Place the test attenuator to the slotted line and detector mount at the other port of test attenuator. Record the reading of

   VSWR meter or on CRO. Let it be P3 then the attenuation value of variable attenuator for particular position of micrometer reading of will be P1-P3 db.
7. In case the variable attenuator change the micro meter reading and record the VSWR meter or CRO reading. Find out attenuation value for different position of micrometer reading and plot a graph.
8. Now change the operating frequency and all steps should be repeated for finding frequency sensitivity of fixed and variable attenuator.

Note:1. For measuring frequency sensitivity of variable attenuator the position of micrometer reading of the variable attenuator should be same for all frequencies of operation.

EXPECTED GRAPH:



OBSERVATION TABLE:

Micrometer reading	P1 (dB)	P2 (dB)	Attenuation = P1-P2 (dB)

RESULT:

EXPERIMENT 13

MICROWAVE FREQUENCY MEASUREMENT

AIM: To determine the frequency and wavelength in a rectangular wave guide working in TE_{10} mode.

EQUIPMENT REQUIRED:

1. Klystron tube
2. Klystron power supply 5kps – 610
3. Klystron mount XM-251
4. Isolator XI-621
5. Frequency meter XF-710
6. Variable attenuator XA-520
7. Slotted section XS-651
8. Tunable probe XP-655
9. VSWR meter SW-115
10. Wave guide stand XU-535
11. Movable Short XT-481
12. Matched termination XL-400

BLOCK DIAGRAM

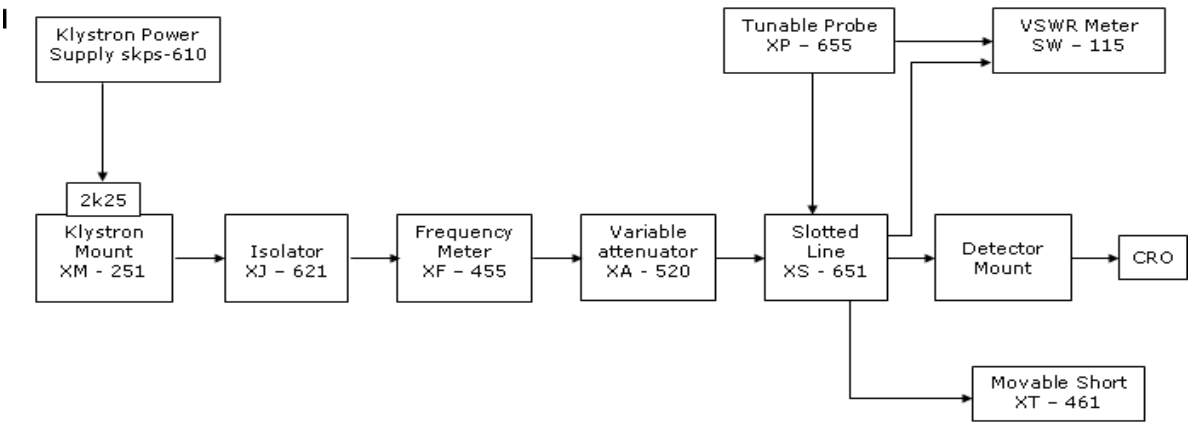


FIG: SET UP FOR FREQUENCY AND WAVELENGTH MEASUREMENT

THEORY:

The cut-off frequency relationship shows that the physical size of the wave guide will determine the propagation of the particular modes of specific orders determined by values of m and n. The minimum cut-off frequency is obtained for a rectangular wave guide having dimension a>b, for values of m=1, n=0, i.e. TE_{10} mode is the dominant mode since for TM_{mn} modes, n#0 or n#0 the lowest-order mode possible is TE_{10}, called the dominant mode in a rectangular wave guide for a>b.

For dominant TE_{10} mode rectangular wave guide λo, λg and λc are related as below. $1/\lambda o^2 = 1/\lambda g^2 + 1/\lambda c^2$

Where λo is free space wave length λg is guide wave length

λc is cut off wave length

For TE_{10} mode λc – 2a where 'a' is broad dimension of wave guide.

PROCEDURE:

1. Set up the components and equipments as shown in figure.
2. Set up variable attenuator at minimum attenuation position.
3. Keep the control knobs of klystron power supply as below:

   Beam voltage – OFF Mod- switch – AM

   Beam voltage knob – Fully anti clock wise Reflector voltage – Fully clock wise

   AM – Amplitude knob – Around fully clock wise AM – Frequency knob – Around mid position
4. Switch 'ON' the klystron power supply CRO and cooling fan switch.
5. Switch 'ON' the beam voltage switch and set beam voltage at 300V with help of beam voltage knob.
6. Adjust the reflector voltage to get the maximum amplitude in CRO
7. Maximize the amplitude with AM amplitude and frequency control knob of power supply.
8. Tune the plunger of klystron mount for maximum Amplitude.
9. Tune the reflector voltage knob for maximum Amplitude.

10. Tune the frequency meter knob to get a 'dip' on the CRO and note down the frequency from frequency meter.
11. Replace the termination with movable short, and detune the frequency meter.
12. Move the probe along with slotted line. The amplitude in CRO will vary .Note and record the probe position , Let it be d1
13. Move the probe to next minimum position and record the probe position again Leti it be d2
14. Calculate the guide wave length as twice the distance between two successive minimum position obtained as above.
15. Measure the wave guide inner board dimension 'a' which will be around 22.86mm for x-band.
16. Calculate the frequency by following equation.

$$f = \sqrt{\left(\frac{c}{\lambda_g}\right)^2 + \left(\frac{1}{\lambda_c}\right)^2}$$

Where C = $3x10^8$ meter/sec. i.e. velocity of light.

17. Verify with frequency obtained by frequency modes
18. Above experiment can be verified at different frequencies. $f_o = C/\lambda o$ => C => $3x10^{10}$ m/s (i.e., velocity of light)

$1/\lambda o^2 = 1/\lambda g^2 + 1/\lambda c^2$

$$\lambda_0 = \frac{\lambda_g \lambda_c}{\sqrt{\lambda_g^2 + \lambda_c^2}}$$

$\lambda g = 2x\Delta_d$

For TE_{10} mode => $\lambda c = 2a$

a □ wave guide inner broad dimension a = 2.286cm" (given in manual)

$\lambda c = 4.6cm$"

RESULT :

EXPERIMENT 14

ANTENNA PATTERN MEASUREMENTS

AIM: Study of wave guide horn and its radiation pattern and determination of the beam width.

EQUIPMENT REQUIRED:

1. Microwave source (Gunn or Klystron) with Power Supply
2. Frequency meter
3. Isolator
4. Variable attenuator
5. Detector mount antennas
6. SWR meter & accessories.

THEORY:

If a transmission line propagating energy is left open at one end, there will be radiation from this end. In case of a rectangular wave-guide this antenna presents a mismatch of about 2:1 and it radiates in many directions. The match will improve if the open wave-guide is a horn shape.

The Radiation pattern of an antenna is a diagram of field strength or more often the power intensity as a function of the aspect angle at a constant distance from the radiating antenna. An antenna pattern is of course three dimensional but for practical reasons it is normally presented as a two dimensional pattern in one or several planes. An antenna pattern consists of several lobes, the main lobe, side lobes and the back lobe. The major power is concentrated in the main lobe and it is required to keep the power in the side lobes arid back lobe as low as possible. The power intensity at the maximum of the main lobe compared to the power intensity achieved from an imaginary omni-directional antenna (radiating equally in all directions) with the same power fed to the antenna is defined as gain of the antenna.

3dB Beam Width :

This is the angle between the two points on a main lobe where the power intensity is half the maximum power intensity.

When measuring an antenna pattern, it is normally most interesting to plot the pattern far from the antenna.

Far field pattern is achieved at a minimum distance of

$$\frac{2D^2}{\lambda_0}$$ - (for rectangular Horn antenna)

Where
D is the size of the broad wall of horn aperture
λ_0 is free space wave length.

It is also very important to avoid disturbing reflection. Antenna measurement are normally made at outdoor ranges or in so called anechoic chambers made of absorbing materials.

Antenna measurements are mostly made with unknown antenna as receiver. There are several methods to measure the gain of antenna. One method is to compare the unknown antenna with a standard gain antenna with known gain. Another method is to use two identical antennas, as transmitter and other as receiver. From following formula the gain can be calculated.

$$P_r = \frac{P_t \lambda_0^2 G_1 G_2}{(4\pi S)^2}$$

Where
P_t is transmitted power P_r

is received Power,

G_1, G_2 is gain of transmitting and receiving antenna S

is the radial distance between two antennas

λo is free space wave length.

If both, transmitting and receiving antenna are identical having gain G then above equation becomes.

$$P_r = \frac{P_t \lambda_0^2 G^2}{(4\pi S)^2},$$

$$G = \frac{4\pi S}{\lambda_0} \sqrt{\frac{P_r}{P_t}}$$

In the above equation P_t, P_r and S and λo can be measured and gain can be computed. As is evident from the above equation, it is not necessary to know the absolute value of P_t and P_r only ratio is required which can be measured by SWR meter.

EXPERIMENTAL SETUP:

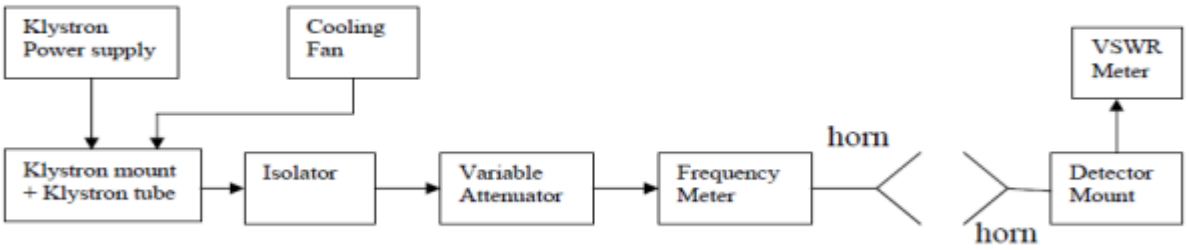


Fig .a. Setup for the Antenna Radiation Pattern measurement

PROCEDURE:

1. Set the equipment as shown in fig. Keeping the axis of both antennas in same line.
2. Initially set the variable attenuator for maximum position.
3. Keep the control knobs of Klystron Power Supply as below: Meter Switch - 'OFF'
4. Mod Switch – AM
5. frequency knob - Around mid position.

(1) Keep the control knob of VSWR meter as below: Meter Switch - Normal
Input Switch - Low Impedance Range
db Switch - 40 db
Gain Control knob - Mid position

(2) Set the equipment as shown in fig. Keeping the axis of both antennas in same line.
(3) Initially set the variable attenuator for maximum position.
(4) Keep the control knobs of Klystron Power Supply as below: Meter Switch - 'OFF'
Mod Switch – AM

Beam voltage knob - Fully anti-clockwise Reflector voltage - Fully clockwise
AM- amplitude knob and frequency knob - Around mid position.
(5) Keep the control knob of VSWR meter as below: Meter Switch - Normal

Input Switch - Low Impedance
Range db Switch - 40 db
Gain Control knob - Mid position)

(5) 'ON' the Klystron Power Supply, VSWR meter and Cooling Fan
(6) Turn the meter switch of power supply to beam voltage position and set beam voltage at 300V with the help of beam voltage knob.
(7) Adjust the reflector voltage to get some deflection in VSWR meter.
(8) Maximize the deflection with AM amplitude and frequency control knob of power supply.
(9) Turn the receiving horn to the left in 5° steps up to 40°- 50° and note the corresponding VSWR db reading in normal db range.
(10) Repeat the above step but this time turns the receiving horn to the right and note down the readings.
(11) Draw a relative power pattern, i.e., output vs. angle.

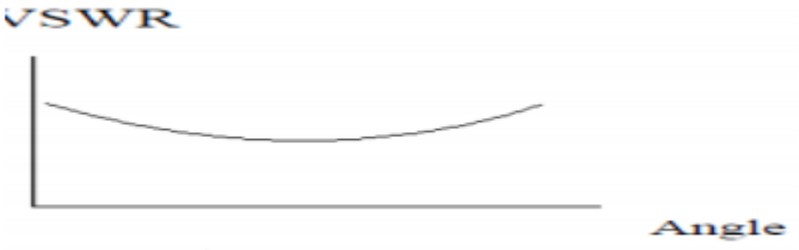
PRECAUTIONS:

1. Use fan to keep the Klystron temperature low.
2. Ensure tight connections of the apparatus
3. Avoid cross connections of the threads.
4. Use stabilized power supply.

OBSERVATION DATA:

S.NO	Angle	VSWR

CHARACTERISTICS:



RESULT & COMMENTS: The radiation pattern is drawn using the values of angle and VSWR.

APPLICATION:

1. Used in television system.
2. Beam width and radiation pattern of horn antenna can be studied.

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Department of Electronics and Communication Engineering

Academic Year: 2019-20 IV B.Tech Semester: I Section-A

Day to Day lab evaluation

Name of the Lab: MICROWAVE ENGINEERING LAB

Roll No.: 17651A0401 **Name of the Student: K Bharath Kumar**

S.No.	Name of the Experiment	Date of Experiment	Record of previous experiment (5 marks)	Execution of experiment (5 marks)	Viva-Voce (5 marks)	Total (15 marks)	Remarks by Faculty
1	Reflex Klystron Characteristics	24.10.2019	5	5	5	15	Excellent
2	Gunn Diode Characteristics	23.7.2019	5	5	5	15	Good work
3	Directional Coupler Characteristics	8.8.2019	5	5	5	15	Good work
4	Measurement of Scattering Parameters of a Magic Tee	31.10.2019	5	5	5	15	Good work
5	Measurement of Waveguide Parameters	8.8.2019	5	5	5	15	Good work
6	Antenna Pattern Measurements.	31.10.2019	5	5	5	15	Excellent
7	Measurement of Scattering Parameters of a E plane Tee	24.10.2019	5	5	4	14	improve for Viva
8	Measurement of Scattering Parameters of a H plane Tee	24.10.2019	5	5	4	14	improve for Viva
9	Antenna Patterns Measurement	31.10.2019	5	5	4	14	improve for Viva
10	Measurement of Scattering Parameters of a Circulator	31.10.2019	5	5	4	14	improve for Viva
11	Attenuation Measurement	19.9.2019	5	5	4	14	improve for Viva
12	Microwave Frequency Measurement	23.7.2019	5	5	4	14	improve for Viva
	Average						

Faculty Member

HOD

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Department of Electronics and Communication Engineering

Academic Year: 2019-20 IV B.Tech Semester: I Section-A

Day to Day lab evaluation

Name of the Lab: MICROWAVE ENGINEERING LAB

Roll No.: 16QM1A0442

Name of the Student: V. Sudhir Goud

S.No.	Name of the Experiment	Date of Experiment	Record of previous experiment (5 marks)	Execution of experiment (5 marks)	Viva-Voce (5 marks)	Total (15 marks)	Remarks by Faculty
1	Reflex Klystron Characteristics	31.10.2019	4	5	4	13	Revise experiments, improve for Viva
2	Gunn Diode Characteristics	8.8.2019	4	5	4	13	Revise experiments, improve for Viva
3	Directional Coupler Characteristics	8.8.2019	4	5	4	13	Revise experiments, improve for Viva
4	VSWR Measurement of Mached load	31.10.2019	4	5	4	13	Revise experiments, improve for Viva
5	Measurement of Waveguide Parameters	8.8.2019	4	5	4	13	Revise experiments, improve for Viva
6	Antenna Pattern Measurements.		4	5	4	13	Revise experiments, improve for Viva
7	Measurement of Scattering Parameters of a E plane Tee		5	5	4	14	improve for Viva
8	Measurement of Scattering Parameters of a H plane Tee		5	5	4	14	improve for Viva
9	Measurement of Scattering Parameters of a Magic Tee	31.10.2019	5	5	4	14	improve for Viva
10	Measurement of Scattering Parameters of a Circulator	31.10.2019	5	5	4	14	improve for Viva
11	Attenuation Measurement	31.10.2019	5	5	4	14	improve for Viva
12	Microwave Frequency Measurement	8.8.2019	5	5	4	14	improve for Viva
	Average						

Faculty Member **HOD**

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Department of Electronics and Communication Engineering

Academic Year: 2019-20 IV B.Tech Semester: I Section-A

Day to Day lab evaluation

Name of the Lab: MICROWAVE ENGINEERING LAB

Roll No.: 16QM1A0439 **Name of the Student: Tanishq choudhary**

S.No.	Name of the Experiment	Date of Experiment	Record of previous experiment (5 marks)	Execution of experiment (5 marks)	Viva-Voce (5 marks)	Total (15 marks)	Remarks by Faculty
1	Reflex Klystron Characteristics	24.10.2019	4	3	3	10	Revise experiments, improve for Viva
2	Gunn Diode Characteristics	31.10.2019	4	3	3	10	Revise experiments, improve for Viva
3	Directional Coupler Characteristics	31.10.2019	4	3	3	10	Revise experiments, improve for Viva
4	VSWR Measurement of Mached load	31.10.2019	4	3	3	10	Revise experiments, improve for Viva
5	Measurement of Waveguide Parameters		4	3	3	10	Revise experiments, improve for Viva
6	Antenna Pattern Measurements.		4	3	3	10	Revise experiments, improve for Viva
7	Measurement of Scattering Parameters of a E plane Tee	24.10.2019	5	5	4	14	improve for Viva
8	Measurement of Scattering Parameters of a H plane Tee	24.10.2019	5	5	4	14	improve for Viva
9	Measurement of Scattering Parameters of a Magic Tee	31.10.2019	5	5	4	14	improve for Viva
10	Measurement of Scattering Parameters of a Circulator		5	5	4	14	improve for Viva
11	Attenuation Measurement		5	5	4	14	improve for Viva
12	Microwave Frequency Measurement		5	5	4	14	improve for Viva
	Average						

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