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Department of Electronics and Communication Engineering

Report of

Value added course on

"Digital Design Using Verilog"

From 12/03/2018 to 16/03/2018

Organized

In collaboration with IETE

by

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COORDINATOR **HOD** **PRINCIPAL**

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THE INSTITUTION OF ELECTRONICS AND TELECOMMUNICATION ENGINEERS
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INDIA

SUMMARY REPORT DIGITAL DESIGN USING VERILOG

About Course

Fundamental of Designers can develop an executable functional specification
that documents the exact behaviour of all the components and their interfaces Designers can make decisions about cost, performance, power, and area earlier in the design process – Designers can create tools which automatically manipulate the design for verification, synthesis, optimization, etc. Hardware description languages are an essential part of modern digital design.

- HDLs can provide an executable functional specification.
- HDLs enable design space exploration early in design process.
- HDLs encourage the development of automated tools.
- HDLs help manage complexity inherent in modern designs.

Scope of the Course

As designs grew larger and more complex, designers began using gate-level models described in a Hardware Description Language to help with verification before fabrication When designers began working on 100,000 gate designs, these gate-level models were too lowlevel for the initial functional specification and early high-level design exploration.

Objectives of the course

Designers again turned to HDLs specification and a framework for help – abstract behavioural models written in an HDL provided both a precise for design exploration Allows designers to talk about what the hardware should do without actually designing the hardware itself, or in other words HDLs allow designers to separate behaviour from implementation at various levels of abstraction

OUTPUT

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The main outputs are mentioned below:

- The expert shared his knowledge among students.
- Students learned from this course and tried to use the techniques for their project as well as research work.
- Students interact with expert to gain their additional knowledge for future research work.
- Students found new ideas, concept, knowledge on technology, different application of methodologies from different session of course.
- Department tried to do their collaborative research work on this course with university as well as industries.
- It was created different domains of research field from this course for possible topic of Electronics and communication Engineering.
- It helped to make industrial project.
- It helped to student for campus recruitment as well as datbase development

Summary of Participants

(a) Number of students attended this course: 031
(b) Number of students certified: 031

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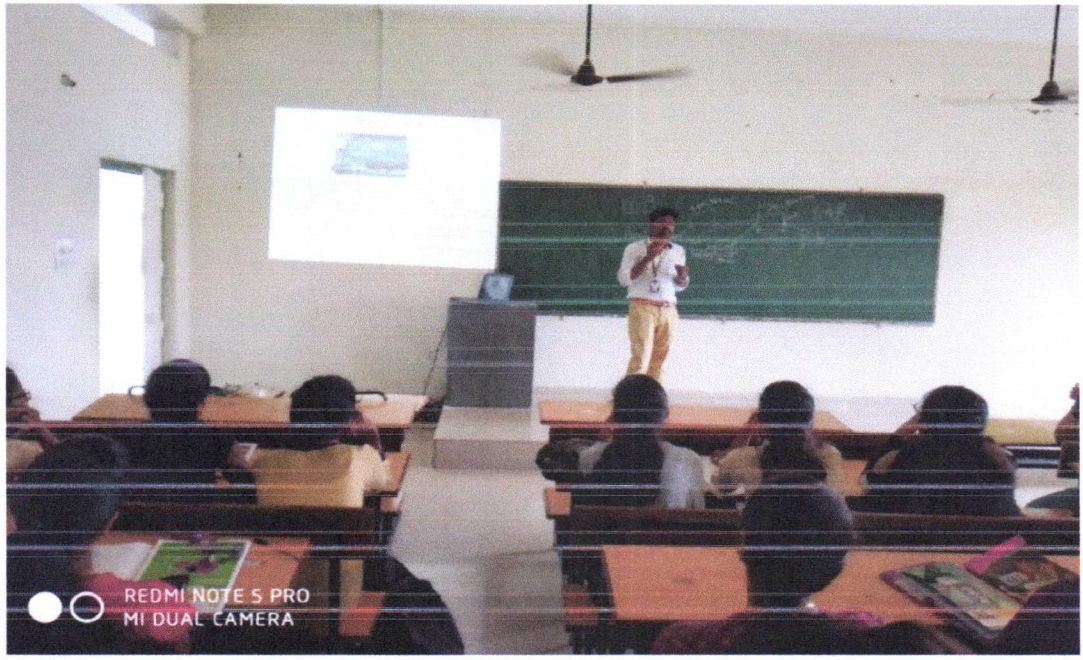
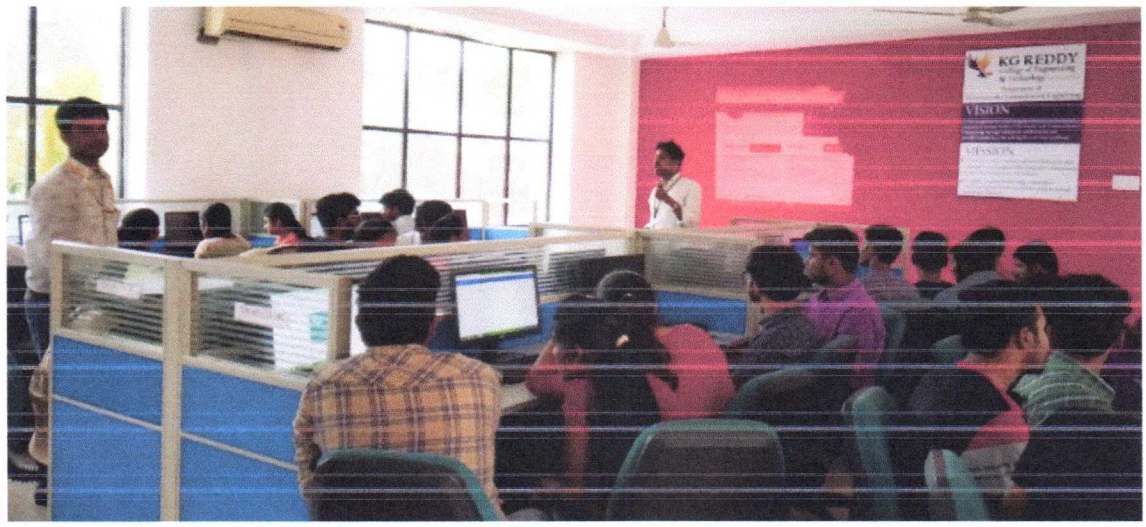
DAY-1:

In the first session students got familiar with Hardware description language and been explained by the expertise. The session was interesting and students run small practical using Xilinx they implemented some circuits on system with simulation.



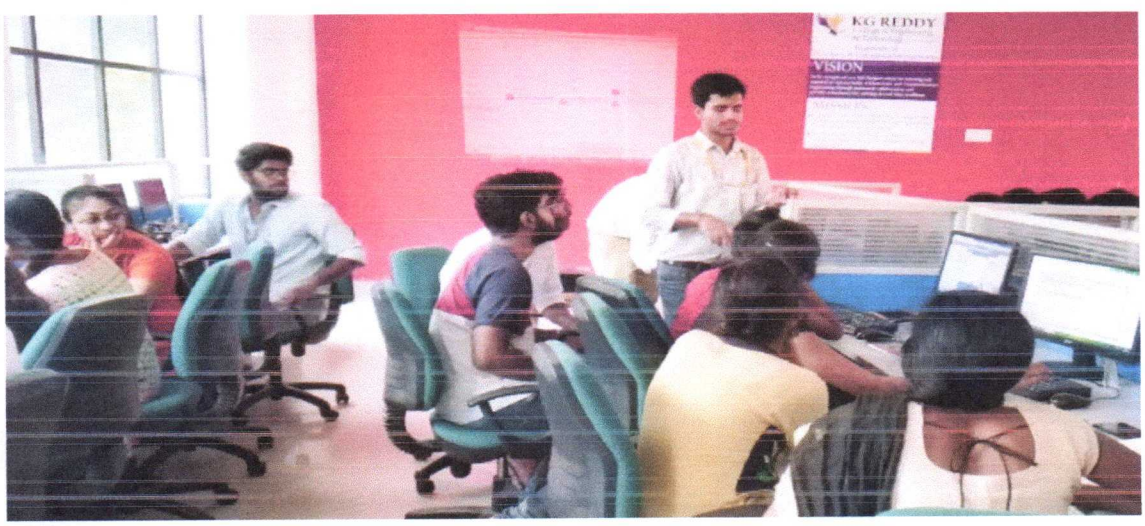
Introduction to Digital Design Using Verilog



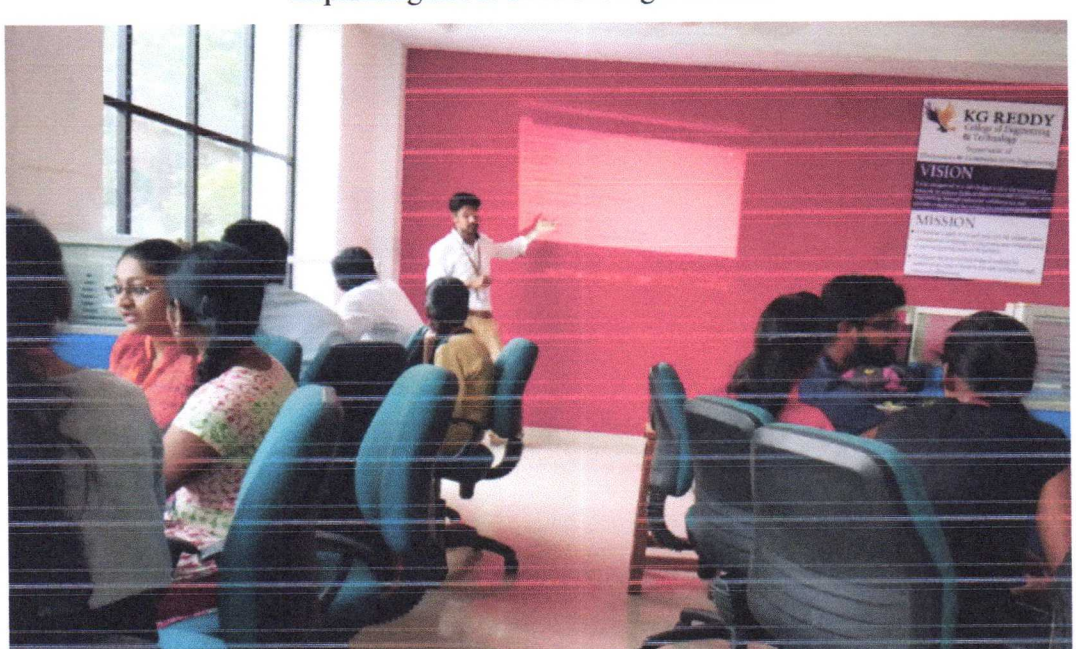
Installation of Xilinx

DAY- 2

In the beginning designs involved just a few gates, and thus it was possible to verify these circuits on paper or with breadboards As designs grew larger and more complex, designers began using gate-level models described in a Hardware Description Language to help with verification before fabrication so different experiments were done using verilog,VHDL programs with the help of expertees.



Explaining about different logic circuits



Explaining the concepts of Verilog and VHDL

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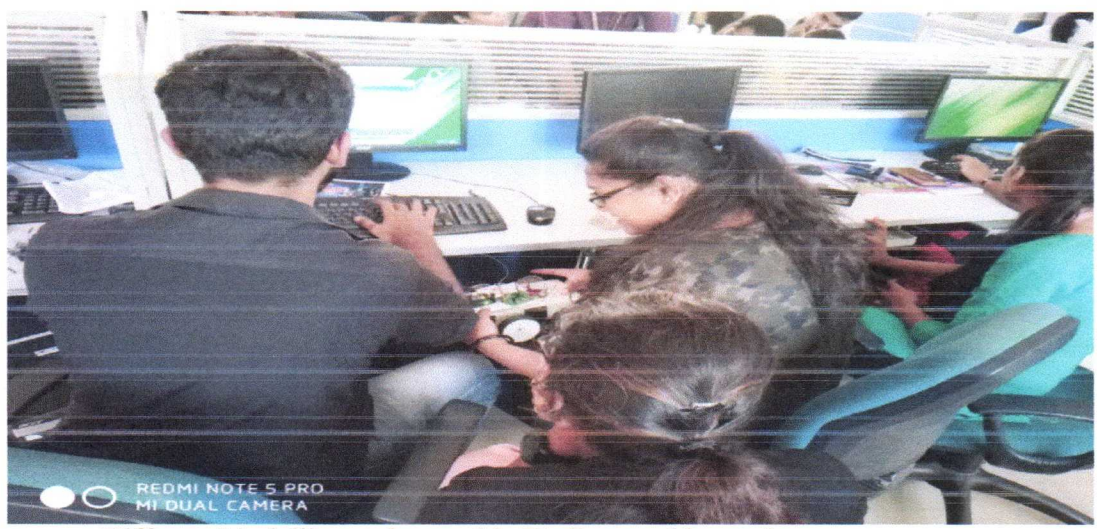
DAY- 3

The following topics have been covered on day 3 that is on Current Trends and role of Programmable logic devices in VLSI Design Industry

- Digital Design concepts & implementation
- Verilog concepts
- Different Modelling styles used in Verilog
- DUT verification by simulation using Directed Test benches
- Synthesizable coding targeted to Xilinx devices
- FPGA Architecture basics
- ASIC & FPGA Design flow
- Synthesis and FPGA Implementation



- Different Modelling styles used in Verilog used by students

DAY- 4

The day 4 was on Digital Design using Logic works following topics have been covered

- Xilinx ISE software for writing HDL codes
- Verifying the HDL codes by writing Testbenches using ISim (Xilinx ISE)
- Synthesis of HDL codes on Xilinx FPGA Kits
- IPCoregen flow
- Xilinx ISE Design flow
- Chipscope Pro flow
- List of FPGA Practicals –Full Adder, Ripple-carry Adder, DFF, Counters, Shifters, ALU, RAM/ROM etc..

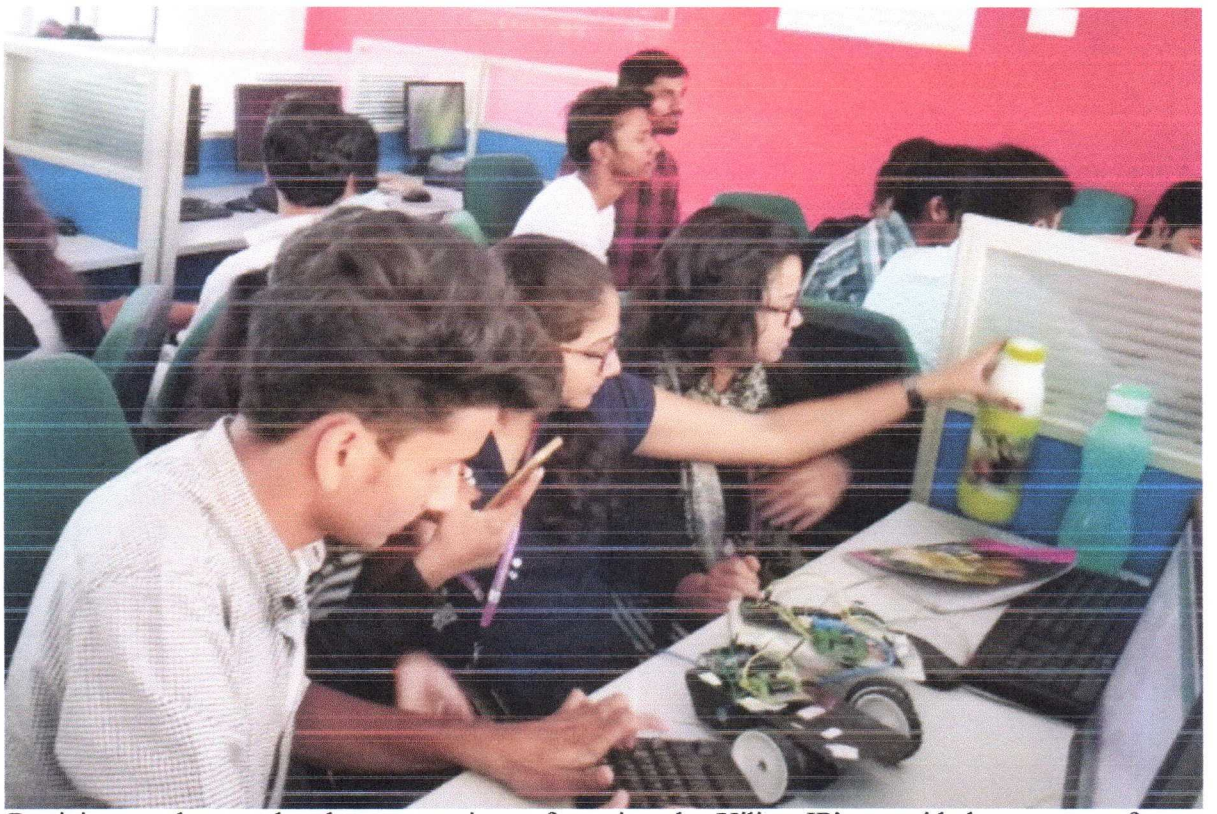
Xilinx ISE software for writing HDL codes and various activity carried out by students

DAY- 5

On the final day Software & Boards Specification and hands on session was carried out by students.

- Logic works 5.0
- Xilinx ISE 14.2 and its associated Tool chain
- Xilinx Spartan 3 and 6 FPGA Development kits

Participants got hands-on experience on Digital Logic Design concepts and implementation, Verilog basics and understanding the powerful features of the language. Participants also got introduced to ASIC vs. FPGA Design flows. They were introduced with the concepts of FPGA internal architecture and finally they also got exposure to the FPGA design flow by themselves synthesizing their own HDL codes into the various development kits from Xilinx.



Participants also got hands on experience for using the Xilinx IP's provided as a part of package in their design

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Ref No: KGRCET/ECE/2017-18/44

CIRCULAR **Date 08 /3/2018**

All the students of II-B.Tech II semester ECE are here by instructed to enroll for the value added course on "**Digital Design Using Verilog**", which is going to conduct from 12/03/2018 to 16/03/2018. Interested students are instructed to meet co ordinator.

HOD

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Syllabus for Digital design using Verilog

Introduction to Digital design using Verilog

Verilog HDL

- Evolution of Computer Aided Digital Design
- Evolution and Importance of Hardware

Description Language (HDL)

- VLSI Design Flow

Basic Concepts of Verilog HDL

- Hierarchical modeling concepts
- Lexical Conventions
- Data Types
- System Tasks and Compiler Directives
- Modules and Ports

Finite State Machine (FSM)

- Introduction to FSM
- State Machine Models and Presentations
- Transition Matrix
- State Transition Diagram
- Moore and Mealy Model
- State Transition Table

Gate Level Modeling

- Gate Types
- Array of Instances
- Gate Delays
- Writing a test bench
- Gate level modeling of various digital circuits

Data flow Modelling

- Continuous Assignments
- Delays
- Operators
- Data Flow modeling of various digital circuits

Behavioural Level Modelling

- Structured Procedures
- Procedural Assignments
- Timing Control
- Conditional Statements
- Multiway Branching
- Loops
- Sequential and Parallel Blocks

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Attendance Sheet for value added course on Digital Design using Verilog

Class:II-II ECE **Date:12/03/2018-16/03/2018**

Sl.No.	Roll No	Name of the Student	Signature				
			12	13	14	15	16
1	16QM1A0401	BALUSANI MANOJ KUMAR					
2	16QM1A0402	BUYYAKER TARUN KUMAR					
3	16QM1A0404	CHEGURI SAI TEJA					
4	16QM1A0406	DIDDE MERCY NIHARIKA					
5	16QM1A0407	GAJJALA CHARITHA REDDY					
6	16QM1A0409	GAVVALA PAVAN KUMAR					
7	16QM1A0410	GONGATI RASHMITHA					
8	16QM1A0412	GURRALA GAYATHRI PADMA KUMARI					
9	16QM1A0414	K SRIVIDHYA					
10	16QM1A0415	KAILASA PRIYANKA					
11	16QM1A0416	KAKULAPATI SESHA SRIVALLI					
12	16QM1A0418	KONIJETI VENKATESH					
13	16QM1A0419	KOTHAPALLI SRIKANTH REDDY					
14	16QM1A0420	KUPPALA VENKATA SAI CHAITANYA					
15	16QM1A0421	M MANIKANTA REDDY					
16	16QM1A0422	MACHABHAVANA					
17	16QM1A0425	MULAKALA BHUVANA SATYA SAI					
18	16QM1A0426	P SAMARA SIMHA REDDY					
19	16QM1A0427	PALNATI CHAITANYA					
20	16QM1A0428	PANGANURU NARESH PHOKRAN					
21	16QM1A0429	PANTHAM KEERTHI					
22	16QM1A0431	R SIMRAN					
23	16QM1A0432	RAJPUT ADITYA SINGH					
24	16QM1A0433	RAMAIAH SUPRIYA					
25	16QM1A0434	RANGAREDDY SAHITHI					
26	16QM1A0435	S SAI SRIVASTHAVA NAIDU					
27	16QM1A0436	SARVIGARI YESHWANTH SIMHA REDDY					
28	16QM1A0438	TALAKANTI MADHURI					
29	16QM1A0439	TANISHQ CHOUDHARY					
30	16QM1A0441	TOTA NARENDRA					
31	16QM1A0442	VOOTKURI SUDHIR GOUD					

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CERTIFICATE

Name: BUYYAKER TARUN KUMAR

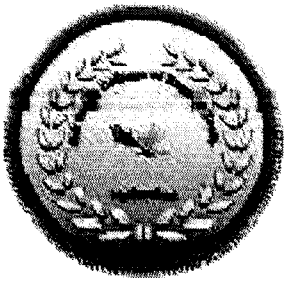
Registration No: 16QM1A0402

has successfully completed the prescribed requirements for the award of value added course on **"Digital Design Using Verilog"** conducted by department of Electronics and Communication Engineering held in month of March from 12/03/2018 to 16/03/2018 in the academic year 2017-2018.

Date: 16-03-2018

Bavu.

Course Coordinator



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CERTIFICATE

Name: CHEGURI SAI TEJA

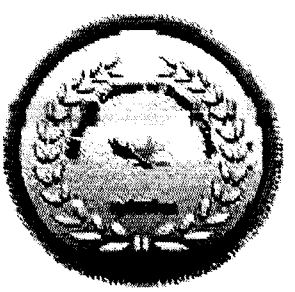
Registration No: 16QM1A0404

has successfully completed the prescribed requirements for the award of value added course on **"Digital Design Using Verilog"** conducted by department of Electronics and Communication Engineering held in month of March from 12/03/2018 to 16/03/2018 in the academic year 2017-2018.

Date: 16-03-2018

Bavu

Course Coordinator



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