KG REDDY
College of Engineering
& Technology

KG REDDY
College of Engineering
& Technology

Department of Electronics and Communication Engineering

Report of

Value added course on

"Digital Design Using Verilog"

From 19/02/2019 to 23/02/2019

Organized

In collaboration with IETE

by

Mr.Bavusaheb B Kunchanur
Assistant Professor
Dept of ECE
KGRCET

Mr. A Vijaya Bhasker Reddy
Assistant Professor
Dept of ECE
KGRCET

COORDINATOR **HOD** **PRINCIPAL**

HEAD
DEPT. OF ELECTRONICS & COMMUNICATIONS ENGINEERING
K.G. REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
CHILKUR (V), MOINABAD, R.R. DIST.501 504.

Principal
KG Reddy College of Engineering & Technology
Chilkur (V), Moinabad (M).
R.R.Dist., Telangana.

THE INSTITUTION OF ELECTRONICS AND TELECOMMUNICATION ENGINEERS • INDIA •
IETE
सह वीर्यं करवावहै

KG REDDY
College of Engineering
& Technology

SUMMARY REPORT DIGITAL DESIGN USING VERILOG

About Course

Fundamental of Designers can develop an executable functional specification
that documents the exact behaviour of all the components and their interfaces Designers can make decisions about cost, performance, power, and area earlier in the design process – Designers can create tools which automatically manipulate the design for verification, synthesis, optimization, etc. Hardware description languages are an essential part of modern digital design.

- HDLs can provide an executable functional specification.
- HDLs enable design space exploration early in design process.
- HDLs encourage the development of automated tools.
- HDLs help manage complexity inherent in modern designs.

Scope of the Course

As designs grew larger and more complex, designers began using gate-level models described in a Hardware Description Language to help with verification before fabrication When designers began working on 100,000 gate designs, these gate-level models were too lowlevel for the initial functional specification and early high-level design exploration.

Objectives of the course

Designers again turned to HDLs specification and a framework for help – abstract behavioural models written in an HDL provided both a precise for design exploration Allows designers to talk about what the hardware should do without actually designing the hardware itself, or in other words HDLs allow designers to separate behaviour from implementation at various levels of abstraction

OUTPUT

Allows designers to talk about what the hardware should do without actually designing the hardware itself, or in other words HDLs allow designers to separate behavior from implementation at various levels of abstraction Allows designers to talk about what the hardware should do without actually designing the hardware itself, or in other words HDLs allow designers to separate behaviour from implementation at various levels of abstraction.

The main outputs are mentioned below:

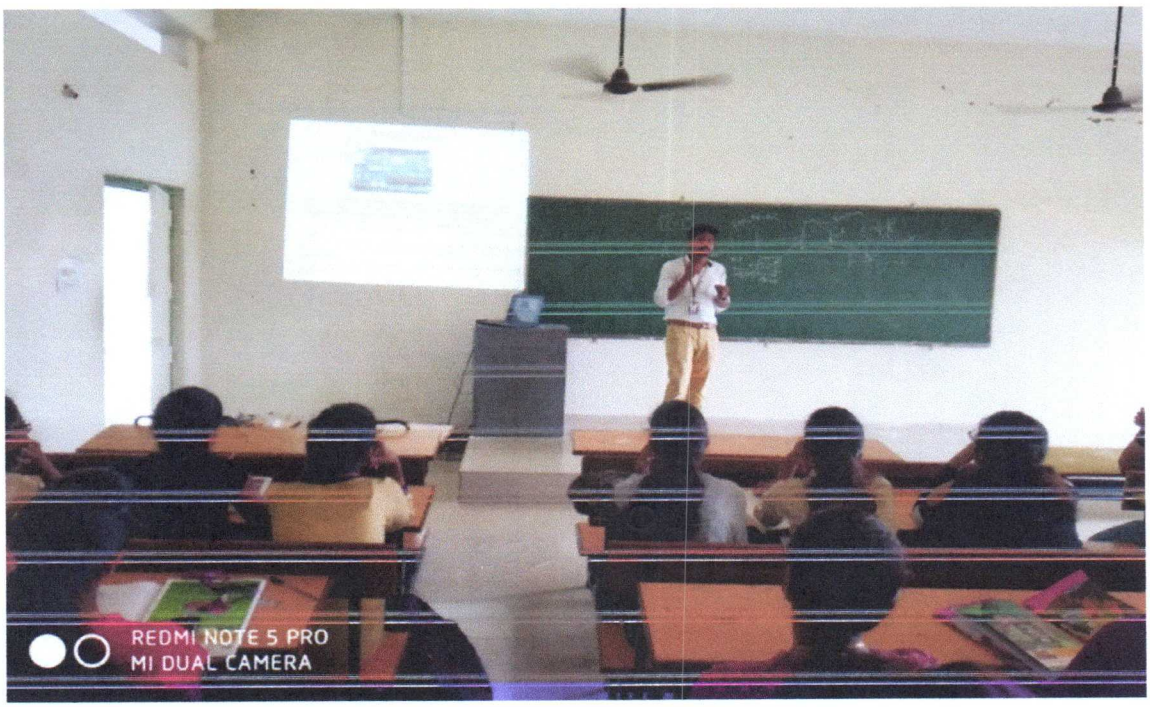
- The expert shared his knowledge among students.
- Students learned from this course and tried to use the techniques for their project as well as research work.
- Students interact with expert to gain their additional knowledge for future research work.
- Students found new ideas, concept, knowledge on technology, different application of methodologies from different session of course.
- Department tried to do their collaborative research work on this course with university as well as industries.
- It was created different domains of research field from this course for possible topic of Electronics and communication Engineering.
- It helped to make industrial project.
- It helped to student for campus recruitment as well as datbase development

Summary of Participants

(a) Number of students attended this course: 052
(b) Number of students certified: 052

DAY-1:

In the first session students got familiar with Hardware description language and been explained by the expertise. The session was interesting and students run small practical using Xilinx they implemented some circuits on system with simulation.



Introduction to Digital Design Using Verilog

DAY- 2

In the beginning designs involved just a few gates, and thus it was possible to verify these circuits on paper or with breadboards As designs grew larger and more complex, designers began using gate-level models described in a Hardware Description Language to help with verification before fabrication so different experiments were done using verilog,VHDL programs with the help of expertees.

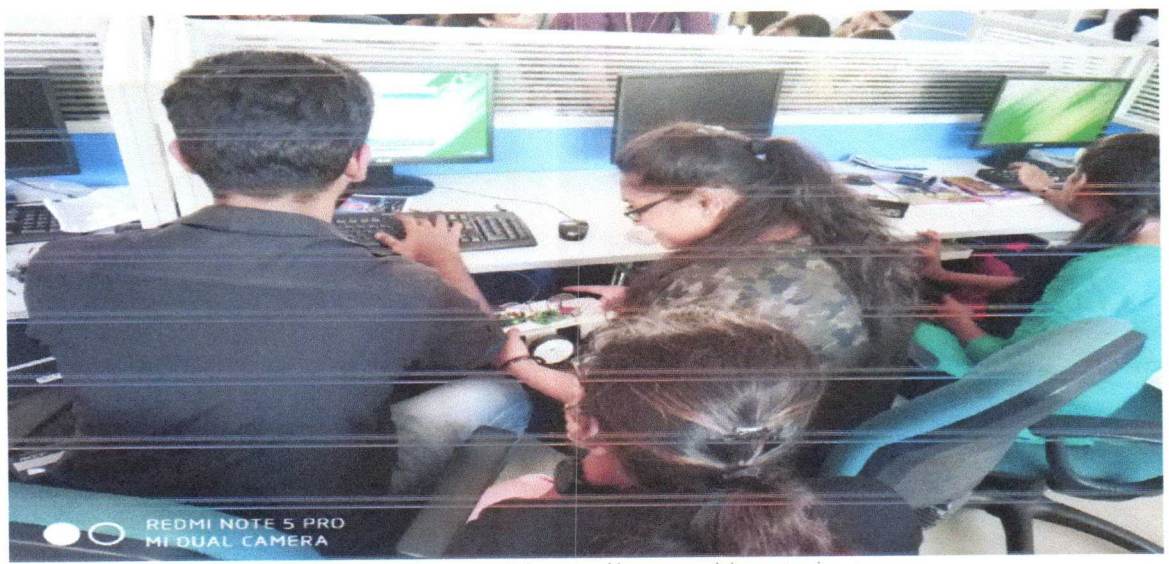
Explaining about different logic circuits

Explaining the concepts of Verilog and VHDL

DAY- 3

The following topics have been covered on day 3 that is on Current Trends and role of Programmable logic devices in VLSI Design Industry

- Digital Design concepts & implementation
- Verilog concepts
- Different Modelling styles used in Verilog
- DUT verification by simulation using Directed Test benches
- Synthesizable coding targeted to Xilinx devices
- FPGA Architecture basics
- ASIC & FPGA Design flow
- Synthesis and FPGA Implementation



- Different Modelling styles used in Verilog used by students

KG REDDY
College of Engineering
& Technology

DAY- 4

The day 4 was on Digital Design using Logic works following topics have been covered

- Xilinx ISE software for writing HDL codes
- Verifying the HDL codes by writing Testbenches using ISim (Xilinx ISE)
- Synthesis of HDL codes on Xilinx FPGA Kits
- IPCoregen flow
- Xilinx ISE Design flow
- Chipscope Pro flow
- List of FPGA Practicals –Full Adder, Ripple-carry Adder, DFF, Counters, Shifters, ALU, RAM/ROM etc..

Xilinx ISE software for writing HDL codes and various activity carried out by students

DAY- 5

On the final day Software & Boards Specification and hands on session was carried out by students.

- Logic works 5.0
- Xilinx ISE 14.2 and its associated Tool chain
- Xilinx Spartan 3 and 6 FPGA Development kits

Participants got hands-on experience on Digital Logic Design concepts and implementation, Verilog basics and understanding the powerful features of the language. Participants also got introduced to ASIC vs. FPGA Design flows. They were introduced with the concepts of FPGA internal architecture and finally they also got exposure to the FPGA design flow by themselves synthesizing their own HDL codes into the various development kits from Xilinx.

Participants also got hands on experience for using the Xilinx IP's provided as a part of package in their design

Students solving realtime problems In the last session, we have conducted a test to evaluate and certify the students At 4:15pm Prof. M.N.Narsaiah, HOD,ECE, KGRCET issued the certificates. He concluded by addressing the students and explained the motive behind the Course. He suggested the students to do their mini, major projects on Arduino and IoT with the help of faculty members.

KG REDDY
College of Engineering
& Technology

Ref No: KGRCET/ECE/2018-19

CIRCULAR **Date 16 /2/2019**

All the students of II-B.Tech II semester ECE are here by instructed to enroll for the value added course on "**Digital Design Using Verilog**", which is going to conduct from 19/02/2019 to 23/02/2019. Interested students are instructed to meet co ordinator

HOD

HEAD
DEPT. OF ELECTRONICS & COMMUNICATIONS ENGINEERING
K.G. REDDY COLLEGE OF ENGINEERING & TECHNOLOGY
CHILKUR (V), MOINABAD, R.R. DIST.501 504.

Principal

Principal
KG Reddy College of Engineering & Technology
Chilkur (V), Moinabad (M).
R.R.Dist., Telangana.

Syllabus for Digital design using Verilog

Introduction to Digital design using Verilog

Verilog HDL

- Evolution of Computer Aided Digital Design
- Evolution and Importance of Hardware

Description Language (HDL)

- VLSI Design Flow

Basic Concepts of Verilog HDL

- Hierarchical modeling concepts
- Lexical Conventions
- Data Types
- System Tasks and Compiler Directives
- Modules and Ports

Finite State Machine (FSM)

- Introduction to FSM
- State Machine Models and Presentations
- Transition Matrix
- State Transition Diagram
- Moore and Mealy Model
- State Transition Table

Gate Level Modeling

- Gate Types
- Array of Instances
- Gate Delays
- Writing a test bench
- Gate level modeling of various digital circuits

Data flow Modelling

- Continuous Assignments
- Delays
- Operators
- Data Flow modeling of various digital circuits

Behavioural Level Modelling

- Structured Procedures
- Procedural Assignments
- Timing Control
- Conditional Statements
- Multiway Branching
- Loops
- Sequential and Parallel Blocks

KG REDDY COLLEGE OF ENGINEERING & TECHNOLOGY

Attendance Sheet for value added course on Digital Design using Verilog

Class:II-II ECE **Date:19/02/2019-23/02/2019**

Sl.No.	Roll No	Name of the Student	Signature				
			19	20	21	22	23
1	16QM1A0405	CHINNAPEESARI SNEHA					
2	17QM1A0401	A RAMADEVI					
3	17QM1A0402	AADHA KAMALAKAR					
4	17QM1A0403	ADLA PRIYANKA					
5	17QM1A0404	ALLI GOUTHAMI					
6	17QM1A0405	ANUGU MAHENDER REDDY					
7	17QM1A0406	BANDARI DHARANI					
8	17QM1A0407	BOKKA KEERTHI REDDY					
9	17QM1A0408	C SAI DEEKSHA SAGAR					
10	17QM1A0409	D SWETHA					
11	17QM1A0410	DANDIGEY VASAVI RANI					
12	17QM1A0411	DEEPAK KUMAR SETH					
13	17QM1A0412	DHARMISHETTY SAMHITHA					
14	17QM1A0413	DUDDU DILEEP KUMAR					
15	17QM1A0414	J KARTHIK					
16	17QM1A0415	K AJAY REDDY					
17	17QM1A0416	K SAI KRISHNA REDDY					
18	17QM1A0418	KADIRA SAI POOJITHA					
19	17QM1A0419	KALIKOTA MEGHANA					
20	17QM1A0420	KARETI NAGA SURENDRA					
21	17QM1A0421	KONDOJU SHIVA SAI CHARAN					
22	17QM1A0422	KOWKUNTLA LOKESH REDDY					
23	17QM1A0423	KUMBAM PAVAN KUMAR					
24	17QM1A0424	KUNTALA CHAITANYA KUMAR					
25	17QM1A0425	LINGALA SHIVA KUMAR					
26	17QM1A0426	MALEKEDI SAI RANI					
27	17QM1A0427	MANDAPAKA DILIP					
28	17QM1A0428	MEGHRAJ BHANU					
29	17QM1A0429	MITTA AKHILA					

30	17QM1A0430	MOHAMMED ZUBAIR KHAN					
31	17QM1A0431	PANTHAM DIVYA					
32	17QM1A0432	PASUPULA MAHESH					
33	17QM1A0433	PUTTA SRAVANTHI					
34	17QM1A0434	RAMAVATH RAKESH NAIK					
35	17QM1A0436	S LILLY MARGRATE MARY					
36	17QM1A0437	S.K GULAM RABBANI					
37	17QM1A0439	SHIVA KUMAR					
38	17QM1A0441	SOMA VIGHNATHA					
39	17QM1A0442	SUNKARI NIKITHA					
40	17QM1A0443	T SAI CHARAN					
41	17QM1A0444	TAMMALI VEERESH					
42	17QM1A0445	THIMMAPURAM MAMATHA					
43	17QM1A0446	TIRMAL APURVA					
44	17QM1A0447	TODUPUNURI AKASH					
45	17QM1A0448	UPPARI DIVYA					
46	17QM1A0449	VISHWANATH VARANASI					
47	17QM1A0450	YALALA PAVANI					
48	17QM1A0451	MOLTHATI YASHWANTH KUMAR					
49	17QM1A0453	MUHAMMED MUSHARRAF UL HAMEED					
50	17QM1A0454	R YASHWANTH					
51	18QM5A0401	BANDARI DATTUKUMARI					
52	18QM5A0402	T RISHI RAJ					
53	176IIA0401	K. Akshaya					

HOD **PRINCIPAL**

54) 1760A0406 G. Ramya Ramya Ramya Ramya Ramya Ramya

HEAD

Principal

KG REDDY
College of Engineering
&Technology

CERTIFICATE

Name: AADHA KAMALAKAR

Registration No: 17QM1A0402

has successfully completed the prescribed requirements for the award of value added course on **"Digital Design Using Verilog"** conducted by department of Electronics and Communication Engineering held in month of February from 19/02/2019 to 23/02/2019 in the academic year 2018-2019.

Date: 23-02-2019

Course Coordinator

Principal

KG REDDY
College of Engineering
&Technology

CERTIFICATE

Name: ADLA PRIYANKA

Registration No: 17QM1A0403

has successfully completed the prescribed requirements for the award of value added course on **"Digital Design Using Verilog"** conducted by department of Electronics and Communication Engineering held in month of February from 19/02/2019 to 23/02/2019 in the academic year 2018-2019.

Date: 23-02-2019

Course Coordinator

Principal