RESUME

Dr. Manisha Guduri
Graduate Member, IEEE (93262232)
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QUALIFICATIONS: **B.Tech** (ECE), **M.Tech** (VLSI System Design) from JNTUH followed by **PhD** in Electronics and Communication Engineering (VLSI design) from BIT, Mesra.

EDUCATIONAL BACKGROUND:

Professional qualification:

Qualification	University/Board	Year of passing	Percentage of marks scored / Grade awarded
PhD (ECE)	BIT, Mesra, Ranchi	2018	8.25/ 1st class with Distinction
M.Tech (VLSI System Design)	JNTUH, Hyderabad	2012	76.3% / 1st class with Distinction
B.Tech (ECE)	JNTUH, Hyderabad	2009	69.3% / 1st class
Other Qualifications – Diploma in Cyber Laws and Intellectual Property Rights	University of Hyderabad, Hyderabad	2022	On-going

Research Projects – Government Funded

DST funded project entitled "A Study on the Constraints in the Growth of Semiconductor Industries in Indian Context" (Fund: 33.684 Lakhs) – Applied – Screened for presentation – Received Approval Letter – Waiting for Sanction Order

DST funded project entitled "Long Term Survival Cardiac Pacemaker – A Low Cost Assistive Device" (Fund: 88.9 Lakhs) – Applied – Screened for presentation – Revision – Waiting for Sanction Order

Industrial Consultancy

Non-Classical CMOS Digital Circuit Design (1.0 Lakh) – On Going

Research & Teaching Experience

4.5 years research experience in BIT Mesra as full time research scholar from 08-03-2014 to 16-07-2018.

11 years teaching experience in various Engineering colleges as Assistant Professor and Associate Professor from July 2009 to June 2010 and May 2011 to Feb 2014 and Jan 2017 till date.

Administrative Roles

4.0 years of experience as **Dean R & D** since 2018 till date.

Head of the department – NBA Coordinator

Highlights of Administrative Roles

1. Initiated MoUs with SR Innovation Exchange, IIIT Hyderabad, Manchester Metropolitan University| John Dalton Building| Chester Street M1 5GD, Manchester, UK
2. Contribution for making National Innovation Startup Policy, Industrial Consultancy Policy, Research Policy
3. During my tenure as Dean R & D, three Research Centers for depts. of ECE, CSE and Mechanical Engineering were approved by JNTUH, Hyderabad.
4. Received Margadarshan from AICTE, New Delhi
5. Received Technology Business Incubator (Nidhi TBI)
6. Recognized by SIRO, DSIR, New Delhi
7. Received 3 Crores of Fund in two years from various funding agencies.
8. Received 88.5 Lakhs of Industrial Consultancy.
9. Got 7.28 RPC in NIRF 2020, which is top in the state of Telangana in Private Engineering Colleges.
10. Good number of research publications in Scopus and SCI (Quality Publications) improved in the institute
11. Applied for ATAL INCUBATION CENTRE (ACIC)
12. Focused towards Intellectual Property Rights – Highest number of Patents in the state of Telangana (IARE as Applicant)
13. Got **NBA** during my tenure as head of the department – NBA Coordinator
14. Key Role in making National Innovation Startup Policy for KG Reddy College of Engineering and Technology, Hyderabad
15. IIC Star Rating improved during my tenure as IIC President from 2.

Intellectual Property Rights

Patent as Inventor:

1. "Thermo Electric static shoes with automatic temperature control ",

Publication date: 15/01/2021, Application No. 202141001091A, IPO, Chennai
2. "Durable Ultra-low Power Cardiac Pacemaker Device", Filing date: 10/01/2021, Application No. 202141001092, IPO, Chennai

Patent as Co – Applicant:

3. Design of Embedded Radiation Hardened Cache Memory Cell, 202141025985, Filed, IPO, Chennai
4. AIGaN/GaN based HEMT for RF and Low Noise Application, 202141025986, Filed, IPO, Chennai

Copy Right – in Process of filing

Impact Factor of Journal Publications

21.942

Research Interest

Broad research area is nanoelectronics.
Research interests include VLSI/CAD design for power- and variability-aware design, design of ultralow-power nanoscale circuits for portable/wearable applications, classical CMOS, non-classical CMOS and non-CMOS (non-Silicon) technologies [which center around the emerging nanoelectronics and devices like HEMT (high electron mobility transistor), FinFET (Fin-Shaped Field Effect Transistor), CNFET (Carbon Nanotube Field Effect Transistor).

Awards

Best paper award in IEEE International Conference on Computational Intelligence & Communication Technology (CICT)

Innovation Ambassador from IIC, Ministry of Education

Recognitions

1. Institution's Innovation Council – President
2. NISP Coordinator
3. Session Chair in IEEE Conference

Other Roles

OBE Committee Member

Institute Newsletter Editorial Board

Member of International Bodies:

1. Graduate Member of IEEE (Membership No. 93262232)

Corporate Life

1. Peer Reviewer in Inderscience Publishers (Springer) – SCI Indexed
2. Peer Reviewer in Multimedia Tools and Applications (Springer) – SCI Indexed
3. Peer Reviewer in IEEE Transactions on VLSI (TVLSI) – SCI Indexed
4. Peer Reviewer in IETE Journal of Research – SCI Indexed
5. Peer Reviewer in Microelectronics Journal – SCI Indexed
6. Reviewer in International Conferences.
7. Convener in Micro2020 – 7th International Conference on Microelectronics, Circuits and Systems on 25th – 26th July 2020, Delhi Technological University, Delhi, India
8. Convener in CCSN 2019 – 8th International Conference on Computing, Communication and Sensor Network- 2019 on 19 Oct – 20 Oct 2019 at Hyderabad, India
9. Member of Organizing Committee (organizing secretary) of International conference of MICRO-2017 (MICRO2017) on 3 Jun – 4 Jun 2017 at Darjeeling, India.
10. Member of Organizing Committee (organizing secretary) of International conference of Computing, Communication and Sensor Network- 2017 (CCSN2017) on 30 Dec – 31 Dec 2016 at Kolkata, India
11. Member of Organizing Committee (organizing secretary) of International conference of Computing, Communication and Sensor Network- 2016 (CCSN2016) on 24 Dec – 25 Dec 2016 at Kolkata, India
12. Member of Organizing Committee (volunteer) of International Conference on Devices, Circuits and Communications (ICDCCom-2014) on 12 Sep – 13 Sept 2014 in BIT Mesra

Invited/Expert Talks/Tutorials

1. Expert talk on "VLSI Design" in technical program organized by Dept. of ECE on 20 Feb. 2017 at Alamuri Ratnamala Institute of Engineering and Technology, Thane, Mumbai, India.
2. Expert Talk on Orientation Session for " Effective Way of Writing a Research Proposal", organized by Centre for Research Innovation and Development on 10th June 2021 at KG Reddy College of Engineering and Technology, Hyderabad, Telangana, India
3. Talk on NBA inspection guidance to DY Patil Institute of Management, Pune on 18th August 2021
4. Expert talk on "Assistive Technologies for Divyangjan" on 26th March 2022 at VR Sidhartha Engineering College, Vijayawada, Andhra Pradesh, India.

Faculty Development Programs Organized

1. One Week Faculty Development Program on "Writing a Research Paper", organized by Centre for Research Innovation and Development from 10th to

16th May 2021 at KG Reddy College of Engineering and Technology, Hyderabad, Telangana, India

2. E- Professional Development Program on "Awareness on Intellectual Property Rights and Strategies on Technology Commercialization" organized by Centre for Research Innovation and Development in association with Institution's Innovation Council from 20th – 26th June 2021 at KG Reddy College of Engineering and Technology, Hyderabad, Telangana, India

Countries Visited

1. Ni Week 2019, Austin, Texas, USA during 10th – 16th May 2019
2. Ajman University, Sharjah, UAE – QS Ranking during 1st Jan to 8th Jan 2020

Premier Institutions Visited

1. IIT, Hyderabad
2. IIIT, Hyderabad
3. T-Hub
4. IIT, Delhi
5. IIT, Bombay
6. EDII, Ahmedabad
7. NIT Warangal
8. Texas University, USA
9. Ajman university, UAE
10. Aligarh Muslim University, Uttar Pradesh
11. Jamia University, Delhi

YouTube Link https://www.youtube.com/watch?v=ELS0GeNPN48

PUBLICATION BRIEF:

International journal	**11**	**2-Elsevier, 3- Springer, 1-JSTS, (6 in SCI and 04 in SCOPUS, 01 in Google Scholar)**
International conference	**19**	
Book chapter	**08**	
Total publication	**38**	
Total impact factor	**21.942**	
h-index	06	Can be seen from https://scholar.google.com/citations?user=7ocllwYAAAAJ&hl=en
i-10 index	01	------do------
Total citation	≥48	------do------

LIST OF PUBLICATIONS

INTERNATIONAL JOURNAL

S.No	Date	Authors/title with journal name/page nos./vol. /no. date/year of Publication	ISSN/ISBN No.	Refereed /Non refereed	Whether indexed and indexing agency	Impact factor
1	Sept. 20	Arshid Numan, Atal A.S. Gill, Saqib Rafique, Manisha Guduri, Yiqiang Zhan, Balaji Maddiboyina, Lijie Li, Sima Singh, Nam Nguyen Dang, "Rationally engineered nanosensors: A novel strategy for the detection of heavy metal ions in the environment", Journal of Hazardous Materials, 2020, 124493, https://doi.org/10.1016/j.jhazmat.2020.124493. (https://www.sciencedirect.com/science/article/pii/S0304389420324833)	0304-3894	Refereed	**SCI**	**9.038**
2	May. 19	**Manisha Guduri,** Amit Krishna Dwivedi, Sananya Majumder, Riya, Aminul Islam, "An efficient circuit-level power reduction technique for ultralow power applications," Microsystem Technologies, vol. 25, pp. 1689–1697, 2019 Publisher: Springer, https://doi.org/10.1007/s00542-018-4103-z	0946-7076	Refereed	**SCI**	**1.737**
3	Nov. 17	**Manisha Guduri**, Vishesh Dokania, Richa Verma, Aminul Islam, "Minimum Energy Solution for Ultra-low Power Applications," Microsystem Technologies, vol. 25, no. 06, pp.	0946-7076	Refereed	**SCI**	**1.737**

		1823-1831 Publisher: Springer https://doi.org/10.1007/s00542-018-3785-6				
4	Jul. 17	Vishesh Dokania, Richa Verma, **Manisha Guduri**, Aminul Islam, "Design of 10T full adder cell for ultralow-power applications", Ain Shams Engineering Journal, 2017, http://dx.doi.org/10.1016/j.asej.2017.05.004. (http://www.sciencedirect.com/science/article/pii/S2090447917300734)	ISSN 2090-4479	Refereed	**SCI**	**1.949**
5	Nov. 16	**Manisha Guduri**, A. Islam, "Novel Pass-Transistor Logic Based Ultralow Power Variation Resilient CMOS Full Adder" Journal of Semiconductor Technology and Science, vol. 17, no. 02, pp. 302-317, https://doi.org/10.5573/JSTS.2017.17.2.302	1598-1657 (Print) 2233-4866 (Online)	Refereed	**SCI**	**2.654**
6	Jun. 16	**Manisha Guduri**, Rishab Mehra, Pragya Srivastava, Aminul Islam, "Current-Mode Circuit-Level Technique to Design Variation-Aware Nanoscale Summing Circuit for Ultra-Low Power Applications," Microsystem Technologies, vol. 22, no. xx, pp. 1-12 DOI: 10.1007/s00542-016-2994-0 Publisher: Springer	0946-7076	Refereed	**SCI**	**1.737**
7	Mar. 16	**Manisha Guduri**, Amit Krishna Dwivedi, Aminul Islam, "High Vt-Low Leakage FDSOI Device for Ultra-Low Power Operation," Indian Journal of Science and Technology, vol. 9, no. 33, pp. 1-5, Sep. 2016. DOI: 10.17485/ijst/2016/v9i33/99516, Publisher: Indian Society for Education and Environment. http://www.indjst.org/index.php/indjst/article/view/99516**.**	Print ISSN : 0974-6846	**Refereed**	**SCOPUS, WOS**	**1.03**
8	Mar. 16	V. Karthik Reddy, **Manisha Guduri**, N Lakshmi Dheshik Reddy, Peddi Dharani, Santashraya Prasad, A. Islam, " Threshold Voltage Extraction of 220 nm FDSOI Device Using Linear Extrapolation Method," Indian Journal of Science and Technology, vol. 9, no. 34, pp. 1-5, Oct. 2016. DOI: 10.17485/ijst/2016/v9i40/99511, Publisher: Indian Society for Education and Environment, http://www.indjst.org/index.php/indjst/article/view/99511**.**	Print ISSN : 0974-6846	**Refereed**	**SCOPUS, WOS**	**1.03**
9	Oct. 16	**Manisha Guduri,** Aminul Islam, "Analysis of XOR Circuits for Ultralow-Power Applications in Deep Subthreshold Region," Indian Journal of Science and Technology, vol. 9, no. 40, pp. 1-6, Oct. 2016. DOI: 10.17485/ijst/2016/v9i40/99510, Publisher: Indian Society for Education and Environment. http://www.indjst.org/index.php/indjst/article/view/99510.	Print ISSN : 0974-6846	**Refereed**	**SCOPUS, WOS**	**1.03**
10	Jun. 15	**Manisha Guduri**, A. Islam, "Design of 4×4 Wallace Tree Multiplier for Ultralow Power Applications with Hybrid Compressors" International Journal of Applied Engineering Research, vol. 10, no. 55, pp. 3584–3589, Jun. 2015, Publisher: Research India Publications. http://www.ripublication.com/Volume/ijaerv10n55spl.htm	Print ISSN 0973-4562, Online ISSN 1087-1090	**Refereed**	**SCOPUS**	**0**
11	Mar. 15	**Manisha Guduri**, Vivek Kumar Agarwal, A. Islam, "Which is the Best 10T Static CMOS Full Adder for Ultralow-Power Applications?," Journal *of VLSI Design Tools & Technology (JoVDTT),*	**Online ISSN: 2249-474X,**	**Refereed**	Indexed in Google Scholar, etc. SJIF 3.035.	**0**

		vol. 5. No. 1, pp. 45-50, Mar. 2015. http://stmjournals.com/index.php?journal=JoVDTT&page=article&op=view&path%5B%5D=5351,	**Print** ISSN: 2321–6492			
		Total Impact Factor				**21.942**

PERSONAL DETAILS:

FATHER'S NAME	G. Surender Rao	**SEX**	Female
DATE OF BIRTH	30-07-1988	**LANGUAGE PROFICIENCY**	English, Hindi, Telugu
NATIONALITY	Indian		

OTHER TECHNICAL SKILLS:

- ✓ CAD tools:
  - Virtuoso ADE (SPECTRE) & Assura of Cadence Design Systems, Inc., Layout design in cadence, post layout simulations in cadence tools.
  - HSPICE of Synopsys, Inc.
  - Athena & Atlas of Silvaco, Inc.
  - Visual TCAD of Cadre Design Systems
  - Microwind – CMOS layout and simulation tool
  - Xilinx ISE of Xilinx, Inc.
- ✓ Hardware Description Languages: VHDL, Verilog,

NUMBER OF PAPERS UNDER REVIEW:

International Journal: 01; Book Chapter: 2 (accepted, yet to publish)

I hereby declare that all the information given in this resume is true to the best of my knowledge and belief.

Dr. Manisha Guduri