Introduction to Low-power high-performance CMOS digital circuit design

Importance and need of the Technology in Industry

Semiconductor chips have pervaded almost everything from computer processors, laptops, mobile phones, automobiles, TVs, and many home appliances. Therefore, Integrated Circuits (ICs) are always in demand. In reality, we are facing a shortage of semiconductor chips globally, and the IC manufacturing companies are trying to catchup the demand. Therefore, engineers (design, layout, etc.) are always required in IC manufacturing companies. With this vision, the program will start with the background that drive us to the development of state-of-the-art digital VLSI designs, then fundamental and core topics will be discussed in detail at transistor level with hands-on with related CAD tools. Circuit simulations, layout, and required automation through scripting, etc. will be highly encouraged throughout the program. The broad approach of the program is to discuss the digital VLSI design from power, performance, and power-delay optimal designs perspective to understand the different design approaches. Students will be exposed to state-of-the-art scaled technology node to better understand the issues related to scaled nodes. Regular assignments will be given to reinforce the concepts. Quizzes will be designed to test student's understandings on the discussed concepts. Projects may carry out in groups, thereby developing the students' abilities to work in teams.

Learning Outcomes

At the end of the certification program, students will be able to

1. understand the historical background that drive to the development of state-of-the-art VLSI digital circuits, the importance of low power, high-performance and power-delay optimal designs, state of the art design issues in digital circuits, the difference between corner based and statistical variations aware designs.
2. get familiar with the combinational and sequential IC design, role of CAD tools in design flow, logic synthesis and simulations, static timing analysis, logical efforts. Structure of various types of MOS transistors, characteristics of MOS transistors, operation of the MOS transistor, Electrical characteristics of MOS transistors. Basic characteristics of a CMOS inverter followed by its noise margin, switching characteristics of MOS inverters, various delay parameters, different circuit configurations, delays/power estimation of full-adder, MUX, AO/AOI cells, flip-flip, latch, parity checker, priority encoder, multiplier, ALU, and other ISCAS benchmark circuits, etc.
3. understand the various sources of power dissipation. Various mechanism affecting the different leakage components in CMOS circuits. They will be able to understand, how technology scaling is enormously increasing the leakage current, and also the impact of process and operating variations on dynamic/static power dissipation.
4. understand the delays mechanism in circuits, mathematical formulation of delays in CMOS circuits. They will also be able to understand the impact of process and operating variations on propagation delays.

Topics to be Covered

- Analyses of power, delay and noise performances of CMOS digital circuits.
- Apply the knowledge of different logic styles for developing digital building blocks such as Gates, full-adder, multiplexors, AOI, latches and flip-flops.

- Design of combinational circuits using CMOS and pass transistor logic for minimum delay and maximum noise margin performances
- Design of optimal sequential CMOS circuit (such as 8-bit multiplier) for the given load and speed requirements, while ensuring no setup time or hold time violations.
- Impact of CMOS technology scaling (e.g., from 45nm to 16nm) on targeted performance figures (power, delays, etc.) on several standard cells and complex digital circuits (ISCAS benchmark).
- Layout designs of targeted circuits and their performance verification.
- Design automation through scripting.

Duration of the certification program

Training: 9-10 weeks

Schedule of the Program

Week	Topic to be covered	Assignment
Week 1	Background, state-of-the-art VLSI digital circuits, why low power, why high-performance and why power-delay optimal designs, design issues in digital circuits, statistical variations, etc.	
Week 2	Design of combinational circuit design for targeted performances (leakage power, dynamic power, propagation delays), role and familiarity with CAD tools in design flow.	Yes
Week 3	Design of sequential circuits for the targeted performance (leakage power, dynamic power, propagation delays, noise margin, area, etc.)	Yes
Week 4	Design of complex circuits for different technology nodes.	Yes
Week 5	Impact of technology scaling, Impact of process, temperature and supply voltage variations on performance figures.	Yes
Mid-exam 1		
Week 6	Project-1	
Week 7	Project-2	
Week 8	Project-3	
Week 9	Project-4	

List of problem-statements for projects

- Design of a 16-bit single-error-correcting and double-error-detecting (SEC/DED) circuit (c1908, benchmark) in CMOS 45nm technology node. Estimate the leakage power in the circuit. Also show the impact of technology (from 45nm to 22nm) on the leakage power.
- Design of 8-bit ALU (c880) in CMOS 32nm technology (using High-Performance model parameters). Show leakage power is increasing with technology scaling (from 32nm to 16nm).

- Design a 27-channel interrupt controller (c432), and estimate leakage power, total power and propagation delays in targeted circuit. Prove propagation delays and static power are decreasing and increasing respectively with lowering the technology nodes.
- Design of a 4x4 Multiplier to estimate leakage current/power for all input combinations and propagation delays for all possible arc including critical path. Design the layout of your multiplier, clearly indicate the location of each standard cell in the design. Compare your pre- and post-layout results.

Profile of Trainer

Dr. Zia Abbas is currently working as faculty member with the Centre for VLSI and Embedded system Technology (CVEST) at IIIT Hyderabad, India. Dr. Abbas received a Ph.D. degree in Electronics Engineering from the Department of Information Engineering, Electronics and Telecommunications (DIET), Sapienza University of Rome, Italy, and an M. Tech (Gold Medallist) in Electronic Circuit and Systems from India. He was an international recipient of a full fellowship for the Ph.D. program in Engineering (Rank-1) in Italy. He is also a recipient of the Marie Currie fellowship in Germany under the European IAPP research grant. During his research tenure in Europe, he worked on several European research projects, such as MODERN and MANON. His current research interests include low-power VLSI circuits, variation-aware nano-CMOS, and FinFET circuits, high yield VLSI designs, Artificial Intelligence-driven VLSI design, etc. He has more than 17 years of research and academic experience at various global organization. Dr. Abbas has published many research articles in IEEE transactions, Elsevier, Wiley, and Springer journals and several papers in national/ international conferences of repute. He co-founder of Analog Intelligent Designs, Inc, Delaware, USA. He has also co-authored two books and has 8 USA and Indian patents (granted/published/filed) to his credit.